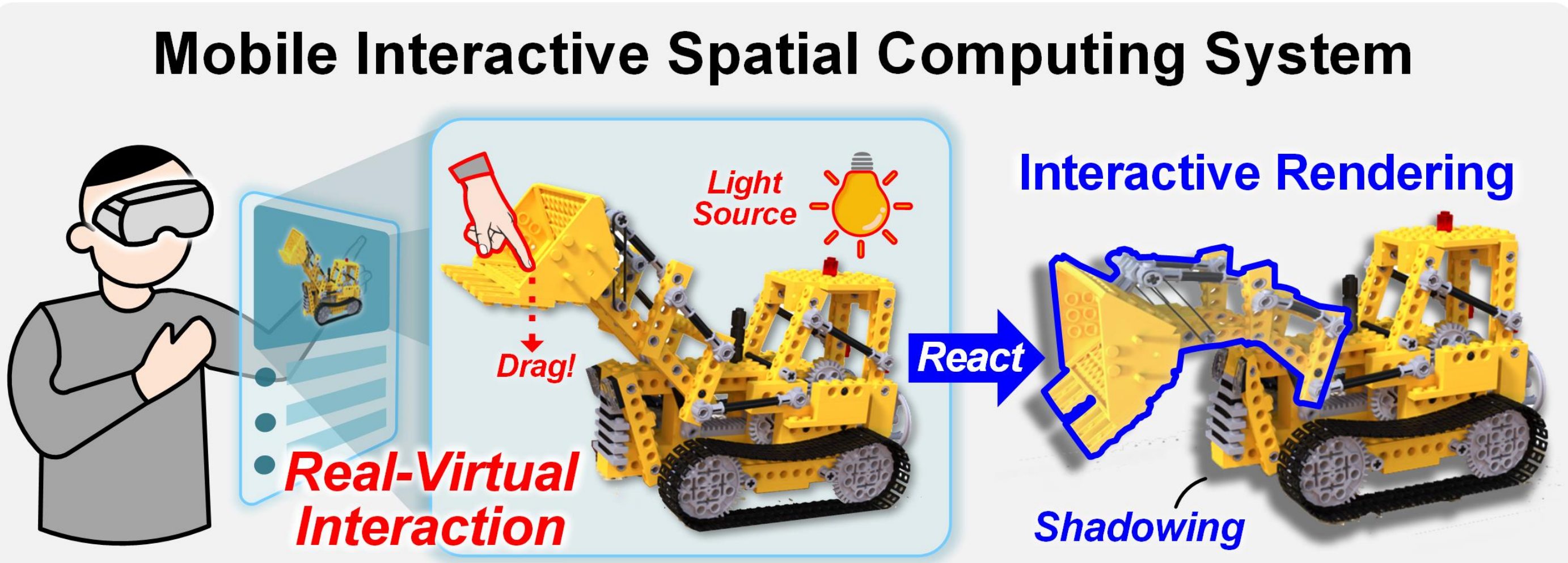


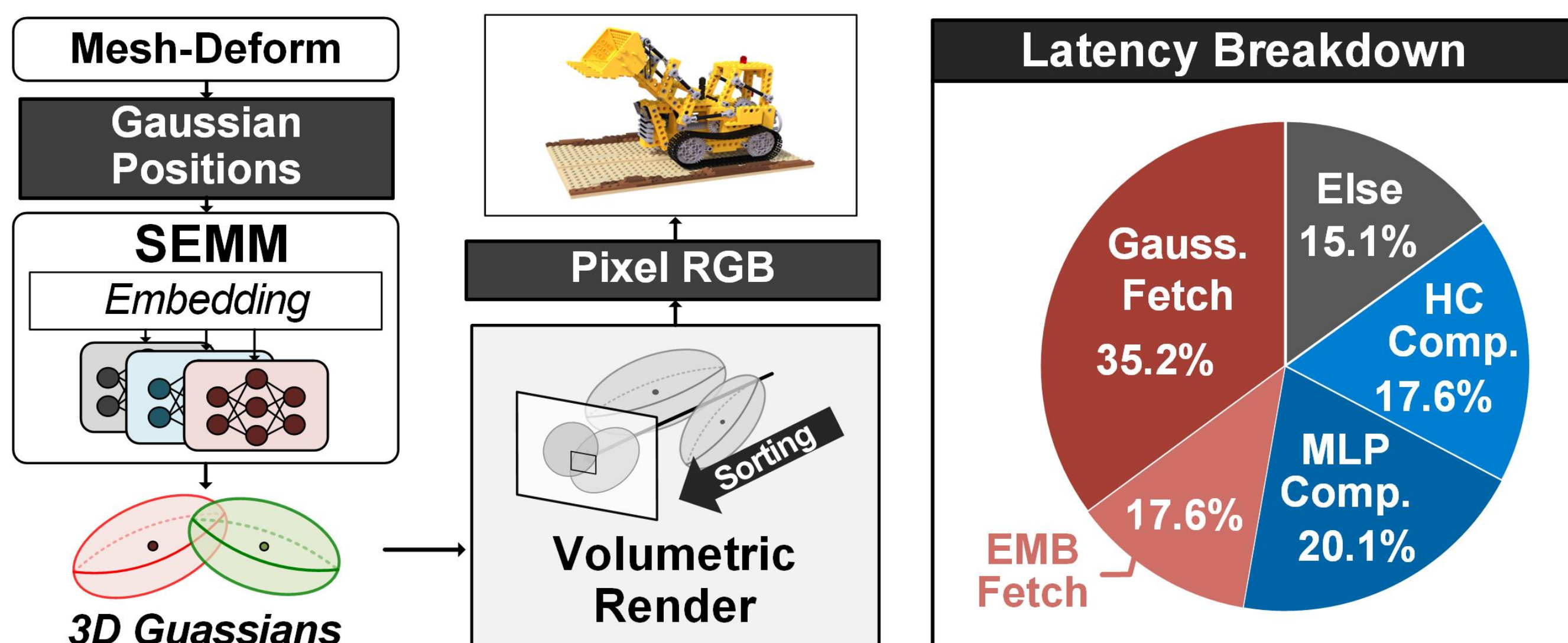
IRIS: A 8.55 mJ/frame Spatial Computing SoC for Real-time Interactable-Rendering and Surface-aware-Modeling with 3D Gaussian Splatting

Seokchan Song, Seryeong Kim, Wonhoon Park, Jongjun Park, Sanghyuk An, Gwangtae Park, Minseo Kim, and Hoi-Jun Yoo (KAIST, Daejeon, South Korea)

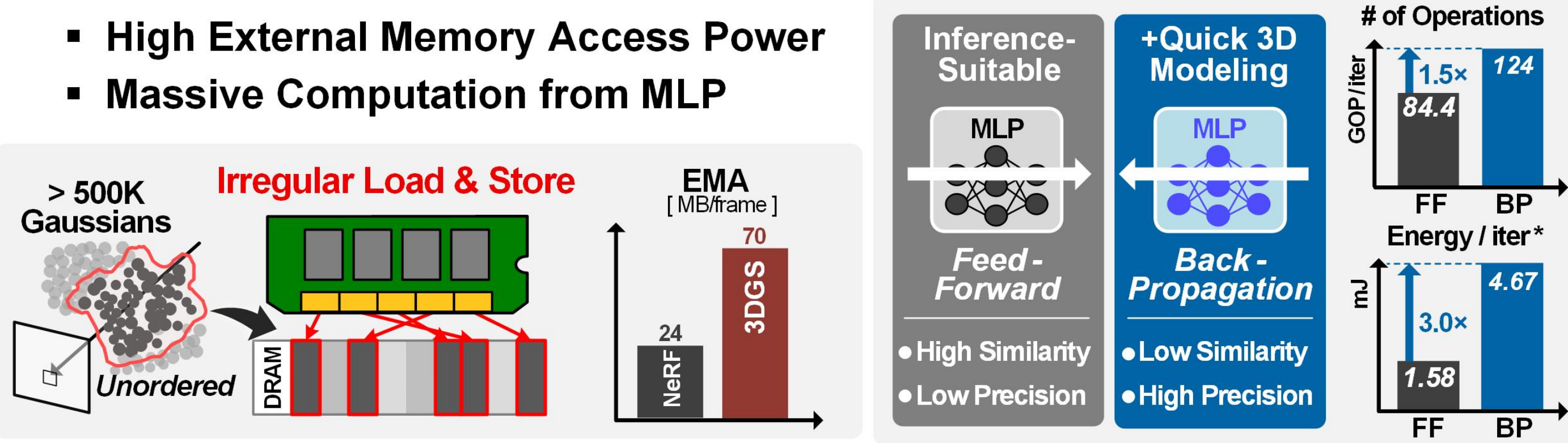
Motivation



Overall Process of Interactive Rendering

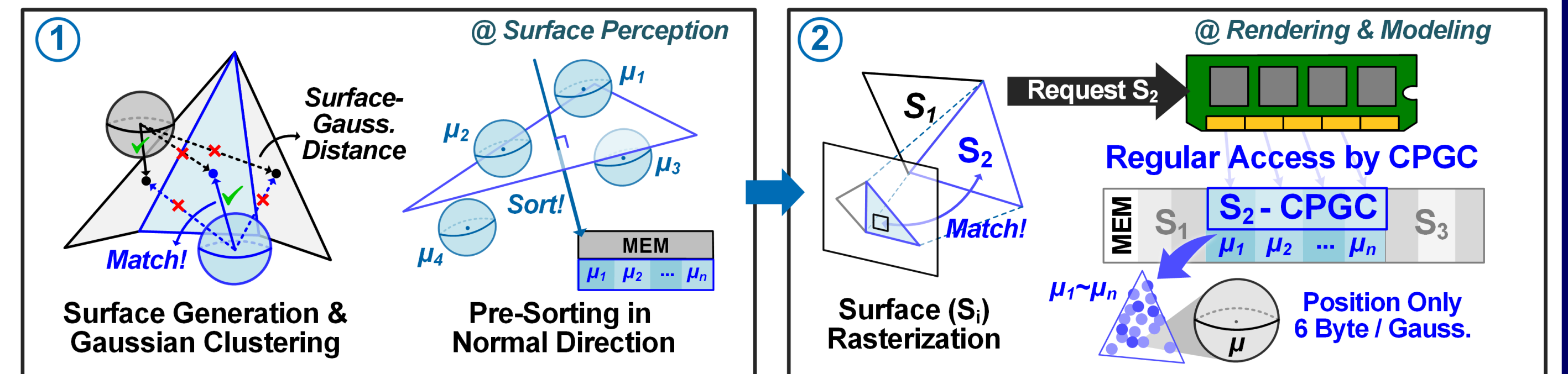


Design Challenges on Mobile AR/VR Devices

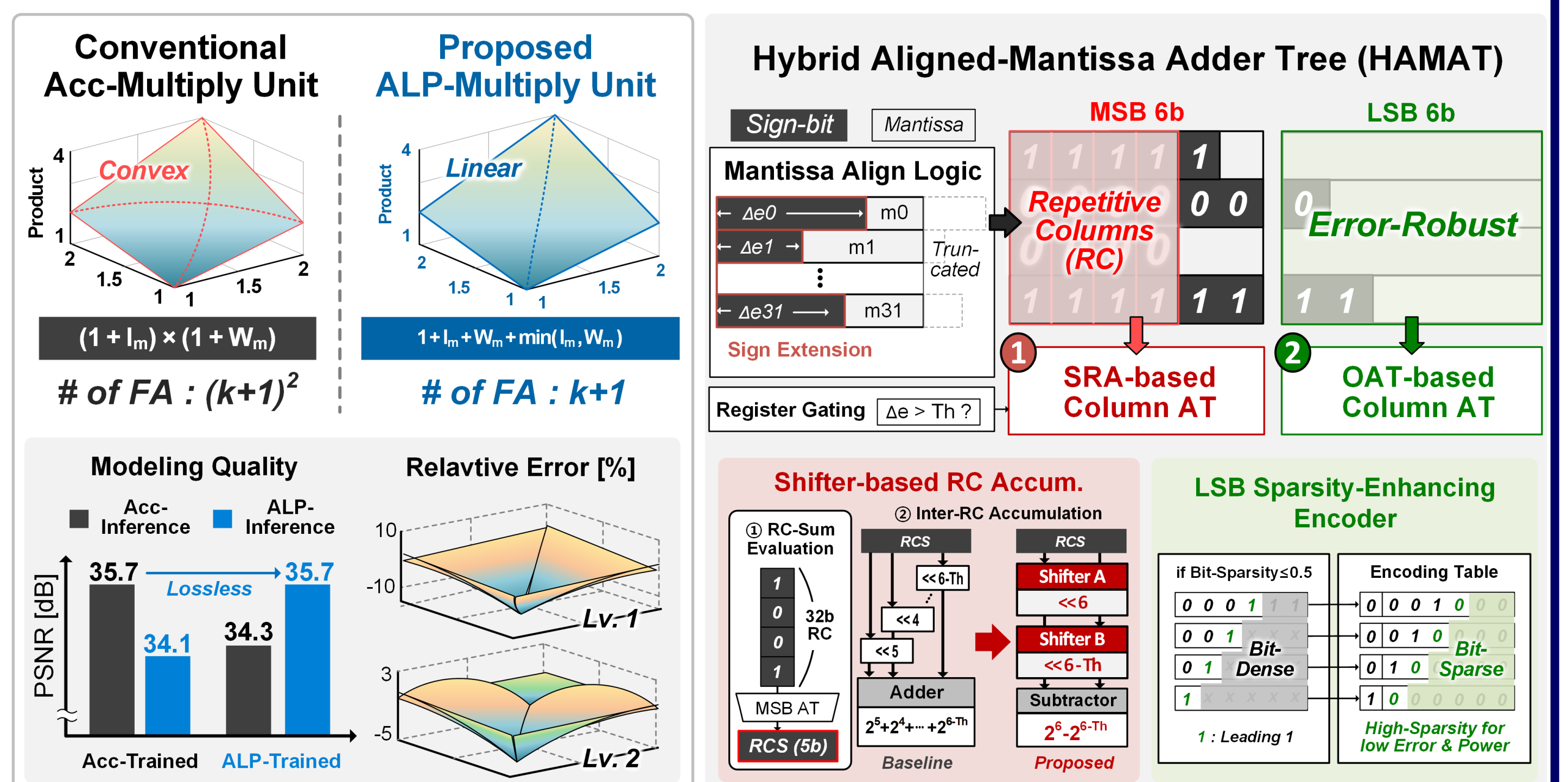


Architecture

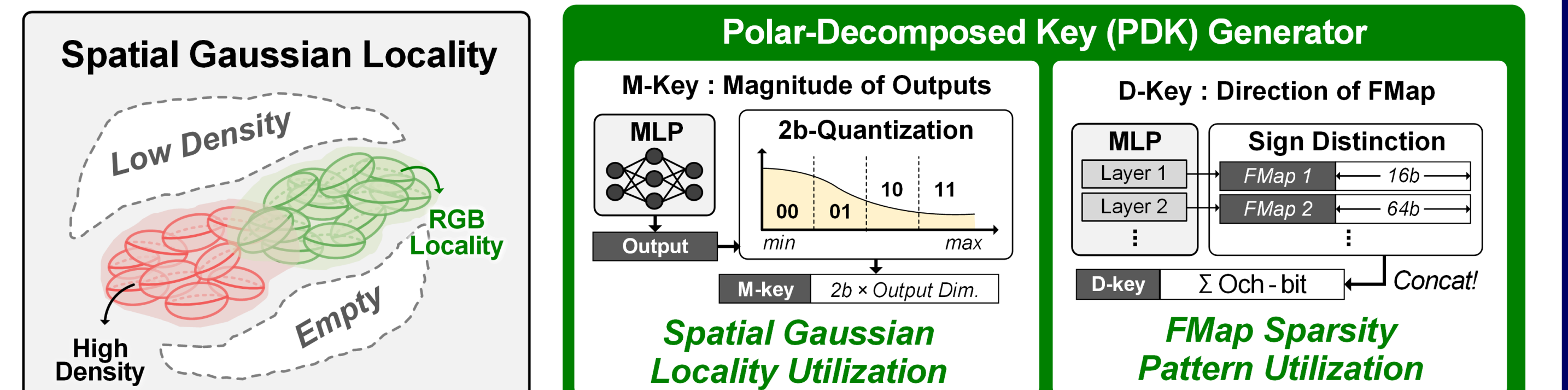
1) Surface Perception Unit w/ Coplanar-Gaussian Cluster (CPGC)



2) ALP-based Reconfigurable Fused MAC Unit

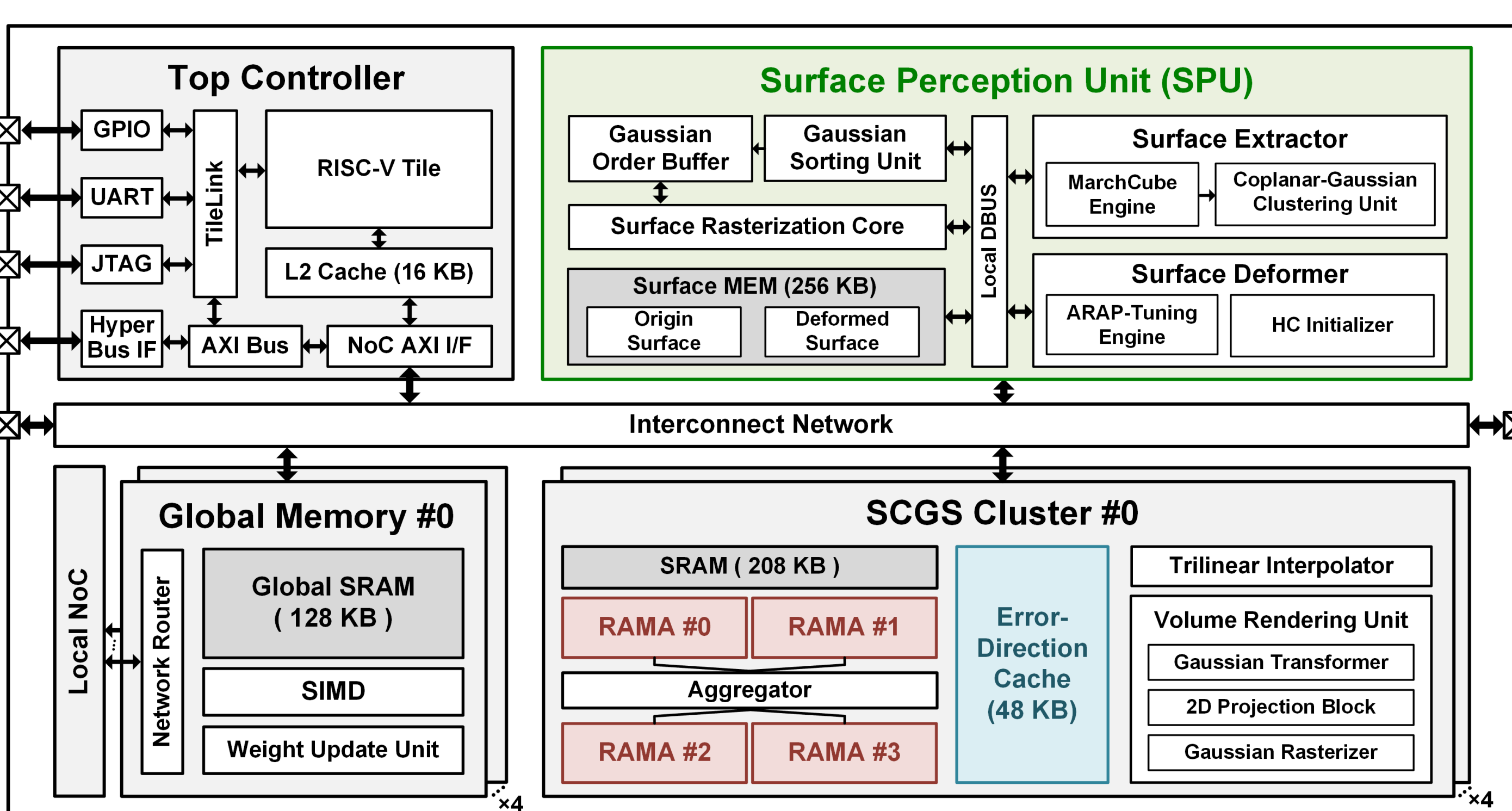


3) ALP-based Reconfigurable Fused MAC Unit



System Implementation

Overall SoC Architecture of IRIS

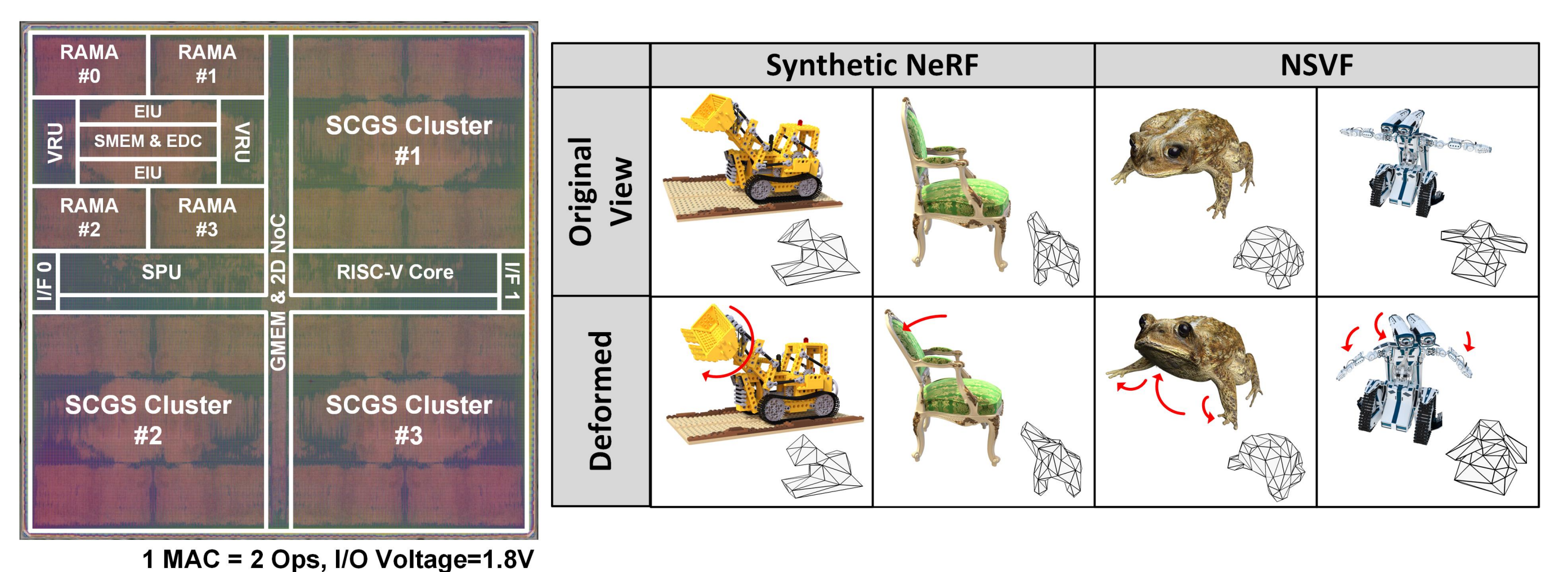


Key Building Blocks of IRIS

- Surface Perception Unit (SPU)**
 - 45.7% **off-chip** memory access latency w/ CPGC
- Reconfigurable ALP-based MAC Array (RAMA)**
 - 2.36x **Area Efficiency** / 2.78x **Energy Efficiency**
 - High Compatibility w/ Reconfigurable Mult Unit
- SEMM-Compressed 3DGS Clusters**
 - 29%p HW utilization enhancement
 - 73% **BP Computation** by Error-Direction Cache

Verification

Chip Summary and Interactive Rendering Results



Demonstration System Implementation & Performance

