High Density Si-IPD Technologies as Enabler for High-Performance and Low-Power Consumption Processor Chips

Mohamed Mehdi Jatlaoui; Jean-Marc Yannou

Murata Integrated Passive Solutions, France

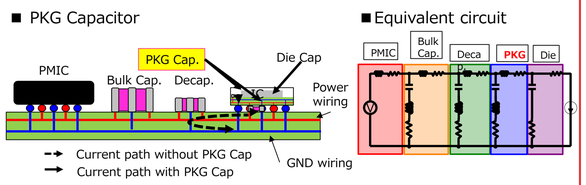
mohamed.jatlaoui@murata.com

Abstract

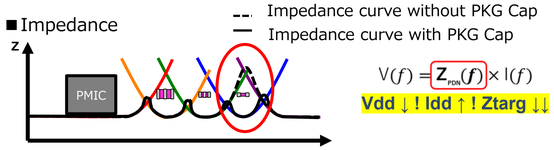
- Voltage regulators are key devices and are part of almost every power electronic system. Indeed, system architects and designers are continuously looking for new topologies and solutions to increase overall efficiency of such devices.
- Thanks to the latest technology advancements in active and passive components, designers were able to achieve amazing performances. This work will present an overview of key breakthroughs in passive components with a focus on Silicon capacitors and IPD (Integrated passive devices).

Introduction

- di/dt Mitigation: Workloads exert excessive load transients and instability in the power supply network: variation in CPU activity may cause droop with steep slopes.



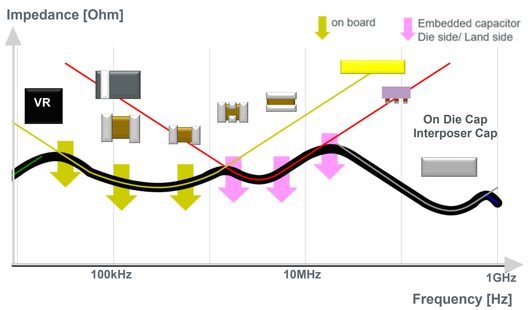
- Higher performance cores switch more current, inducing deeper droops. This impact is amplified at lower operating voltages as required by scaling trends.
- There is a need for an efficient PDN decoupling strategy.



$$V(f) = Z_{PDN}(f) \times I(f)$$

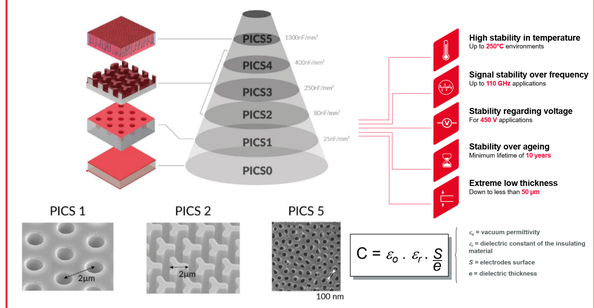
Vdd ↓ ! Idd ↑ ! Ztarg ↓↓

- **To mitigate di/dt, Lower impedance is required**
  - **At intermediate frequency → High C, Low ESR**
  - **At high frequency → Low ESL**

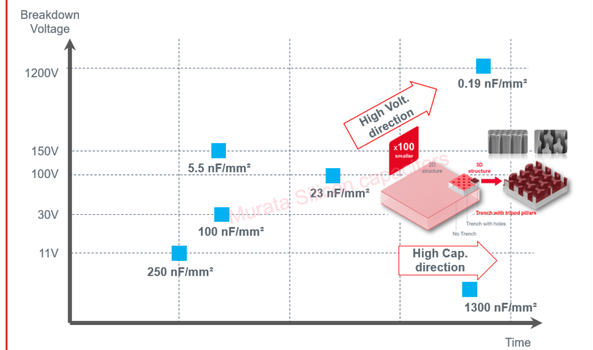


Silicon Capacitor Technology

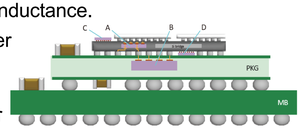
- State-of-the-art 3D structure, featuring a compact and low-profile design with high capacitance density.



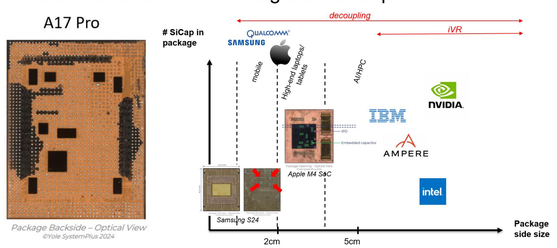
- Technology Roadmap targeting high capacitance density and high voltage.



- Silicon decoupling capacitors are placed very close to the IC minimizing routing parasitic inductance.
- Embedded for (A) : interposer
- (B) : PKG substrate
- (C) : Die side
- (D) : Land side for interposer

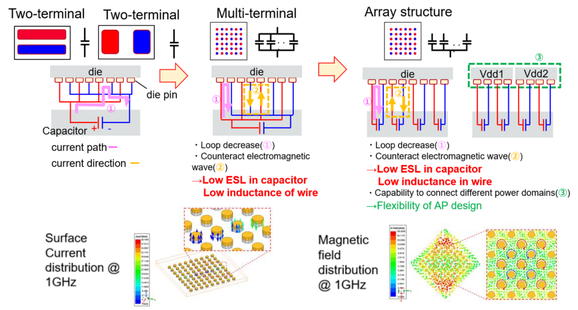


- There is a need for more integrated Si-Cap



Results

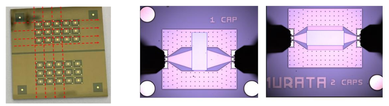
- Optimized capacitor design with multi-terminal connections to minimize the ESL (Equivalent Series Inductance) at package level.
- Multiple capacitors in one single die (capacitor array) enabling multi-power domains decoupling



- Measurement results: Very Low ESR and ESL

Evaluation board

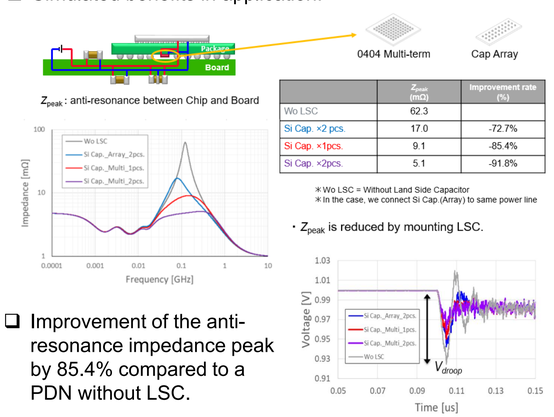
- ✓ SC 256nF
- ✓ SC 512nF
- ✓ SC 1000nF



Measurement Results

	SC256	SC512	SC1000
Configuration	2 caps	4 caps	1 single cap
Cap (nF)	240	506	1000
ESR@SRF (mΩ)	7	4	3
ESL[1] (pH)	4	3	4

- Simulated benefits in application:



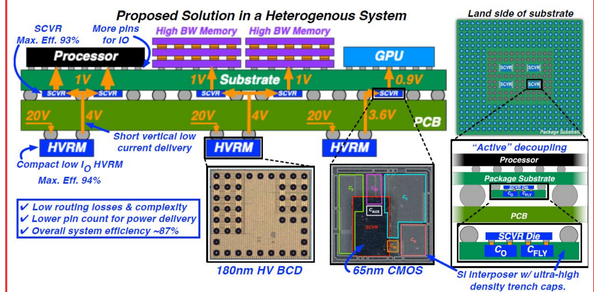
- Improvement of the anti-resonance impedance peak by 85.4% compared to a PDN without LSC.

Conclusion

- Power delivery challenges:
  - Increase computing capability in fixed power budget
  - VDD scaling → drastic drop in impedance: Vdd ↓ ! Idd ↑ ! Ztarg ↓↓
  - Key solution → find the best in-package decoupling strategy for a 3D-IC implementation.
- Silicon capacitor technology enables:
  - Optimized and flat PDN Design: Low ESL, High Density and adjustable ESR.
  - Z_{peak} and V_{droop} improved by using Si-Cap.
  - Advanced packaging solution: Low profile, multi-terminal interconnections, capacitor array structure and minimized bump depopulation.
- Si-cap technology is continually evolving to meet new PDN challenges:
  - High density roadmap to increase the capacitance and reduce size.
  - Flexibility from design and packaging point of view.
  - Silicon capacitor as reference in PDN design with high volume manufacturability and assembly capabilities.
  - Suitable for other power applications: iVR ,…

Future Outlook

Two-Stage Vertical Power Delivery Approach



Vertical Power Delivery with Heterogenous Integration

- New circuit topology and control
- Switched capacitor for the last stage
- Integrated passive devices (IPDs)
- >1 uF/mm²
- Silicon interposer for packaging
- Target: 2 A/mm²
- 87% total efficiency, with 94% for HVRM and ~93% for SCVR
- Ref: C. Hardy et al @ ISSCC 2023

■ This work is supported by: