Hot Chips 2025

Taping Out Three Class Chips Per Semester in Intel 16 Technology

Lucy Revina, Ethan Gao, Ken Ho, Daniel Lovell, Kristofer Pister, Borivoje Nikolić
University of California, Berkeley

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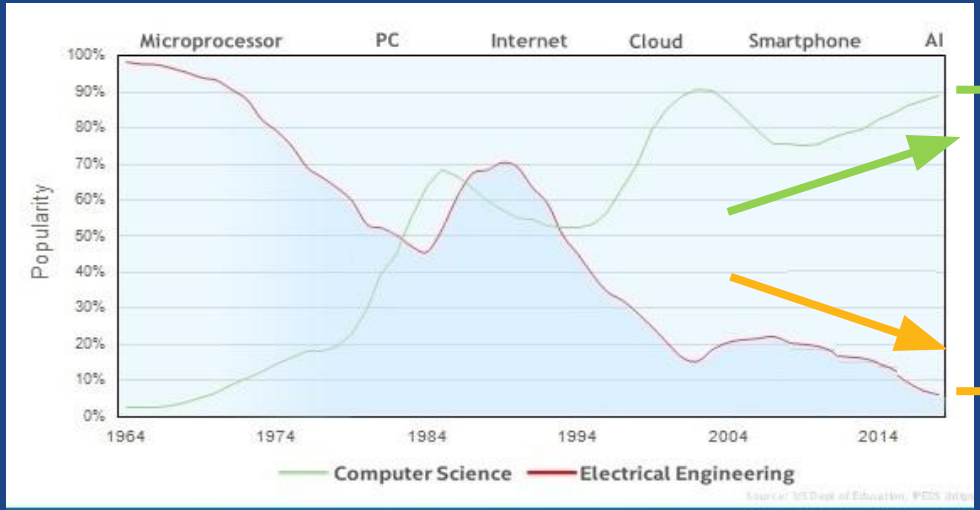
The Golden Age Paradox

"It's a new Golden Age for computer architecture.."
But where are the Golden Age architects? For a while, not many in college:

College Enrollment Interest



Computer Science

Electrical Engineering

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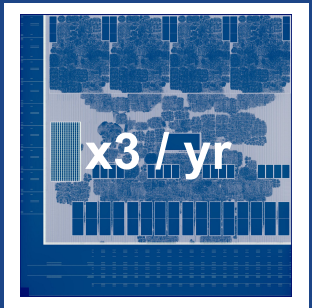
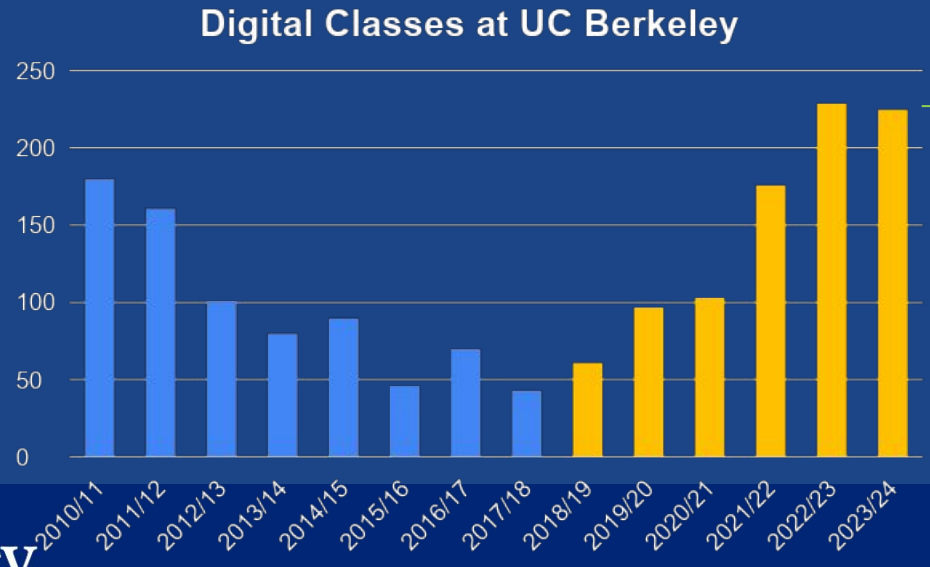
Raja Koduri, VLSI'22
(source: US Dept of Education)

Computer Architecture Revived in the Classroom

We've reversed the trend. Agile chip design with Chipyard is one reason. Students TO real Intel 16 silicon in 15 weeks - we present 3 case studies.





> 200 undergrads,
limited by lab capacity

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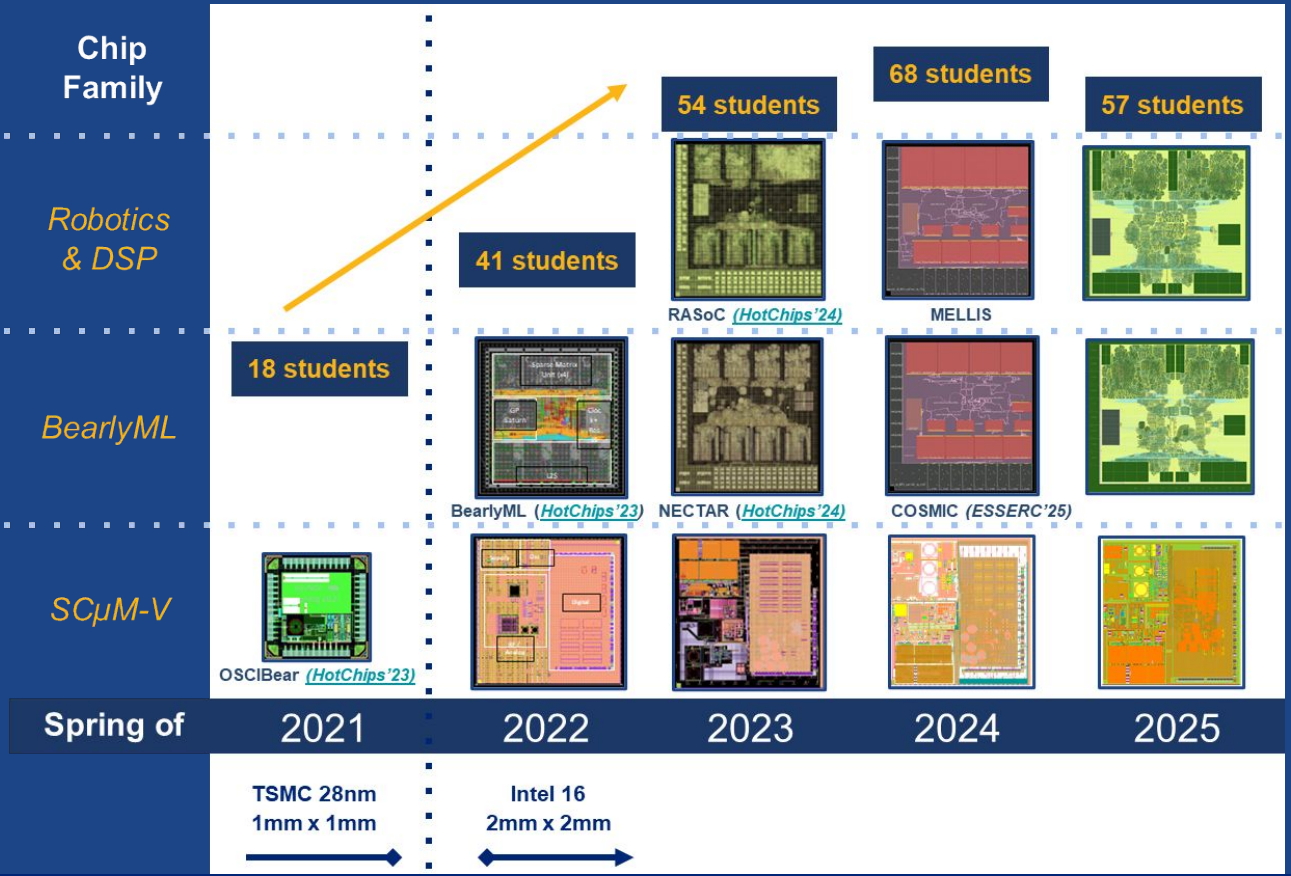
UC Berkeley Enrollment Data

Only The Tip of the Class Chip Iceberg

COSMIC, MELLIS, and SCµM-V24 are preceded by 6 class tapeouts 2021-2024.



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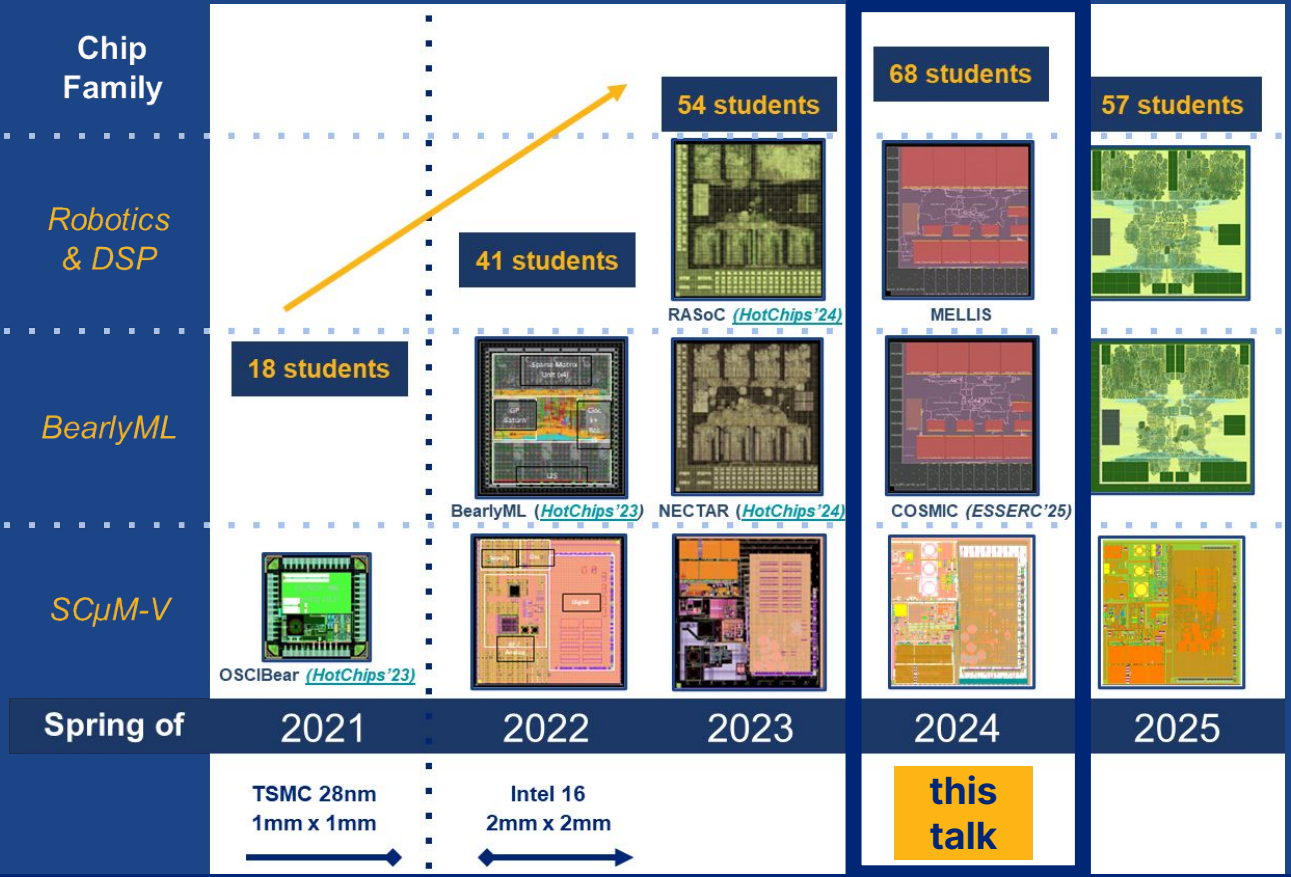

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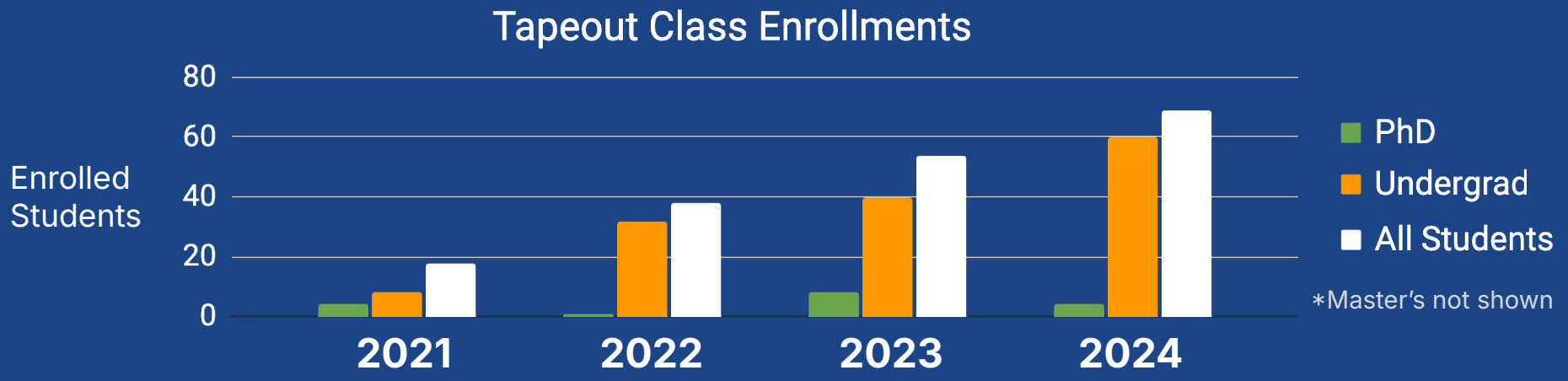
Allure of “the most intense, fun class of my career!”

Started with grad/undergrad students, the class is now 80-90% undergrad.
Majority are from CS - only 1/3 ever took an analog circuits class.



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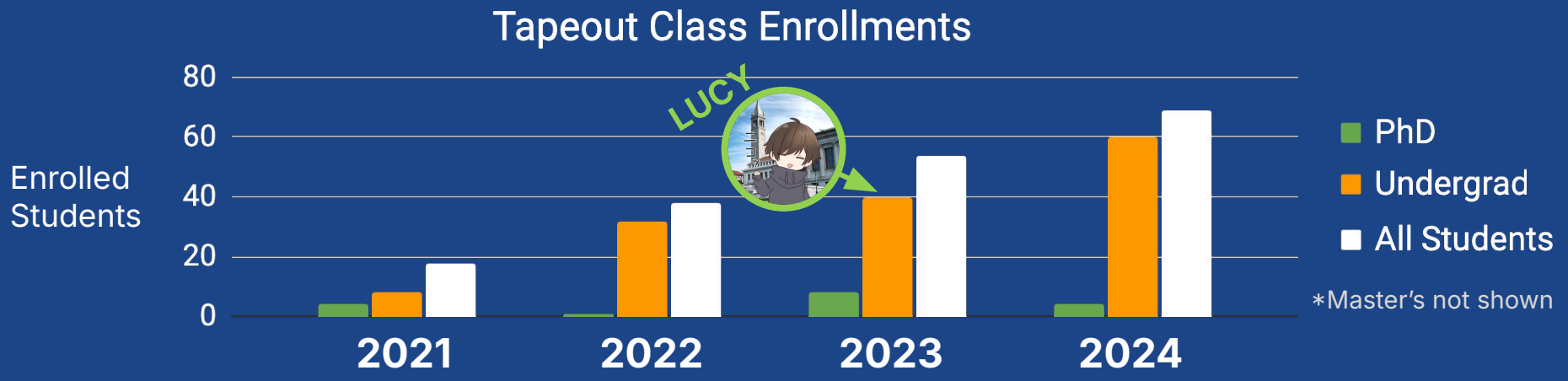
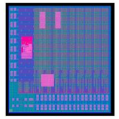


How do we do it?

Two semesters.
A short lab sprint.
Open source HW.
Industry timeline compressed.

	JAN	FEB	MARCH	APRIL	MAY
TAPEOUT	16 Class Starts	"Toy Tapeout"	15 Mock Tapeout 23-31 Spring Break	2 Design Review 11 Mock Tapeout	2 Final Review 10 Submit GDS
	Labs 1 | 2 | 3	Labs 4 | 5	Preliminary RTL Design Freeze	Midterm DRC Clean Design Review	Final Review & Tapeout
SUMMER FABRICATION					
					
	22 Class Starts		"Midterm Review"		12 Industry Review
BRINGUP	AUG	SEPT	OCT	NOV	DEC
	Chip Spec Review & Set Bringup Targets	PCB Practice Lab & Design	Chips Arrive & 0-Day Bringup Sprint	PCBs Return Baremetal Code Lab	Final Review & Demos

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The Not-So-Secret Framework Sauce

Chipyard: Agility through configurable generators.

Chisel: Scala-based HDL.

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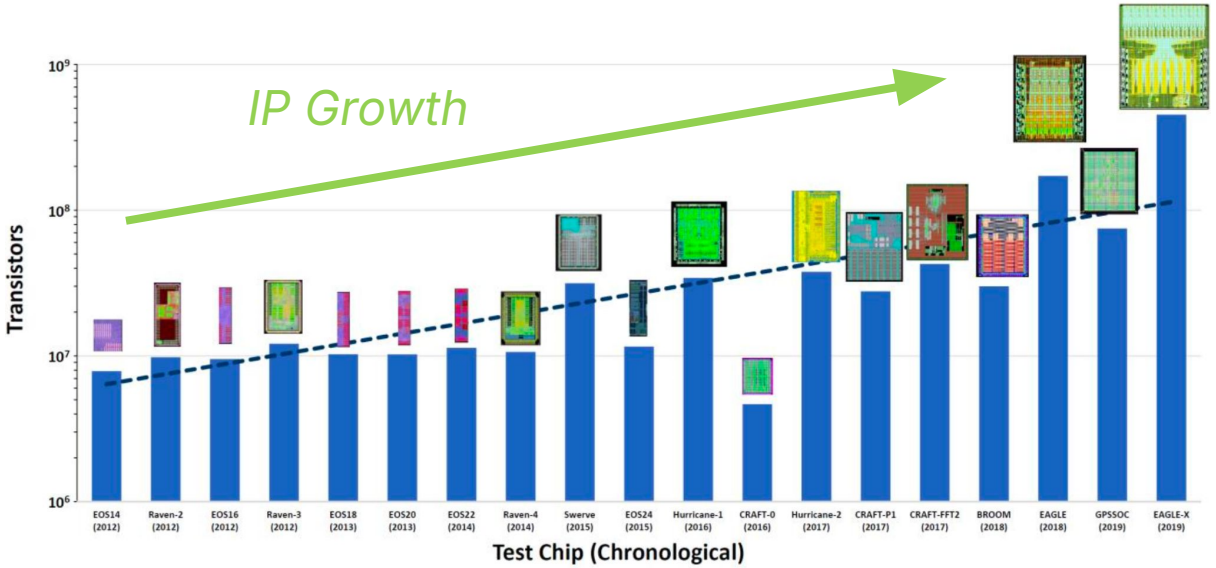
CHIPYARD



https://github.com/chipsalliance/chisel J. Bachrach et al., DAC 2012
https://github.com/ucb-bar/chipyard/ A. Alon, et al., IEEE Micro 2020

What is Chipyard?

SoC / SiP design tools and software.

Curated IP library of open-source RISC-V SoC components.

End-to-end methodology for agile architecture exploration, design, PD, and evaluation.

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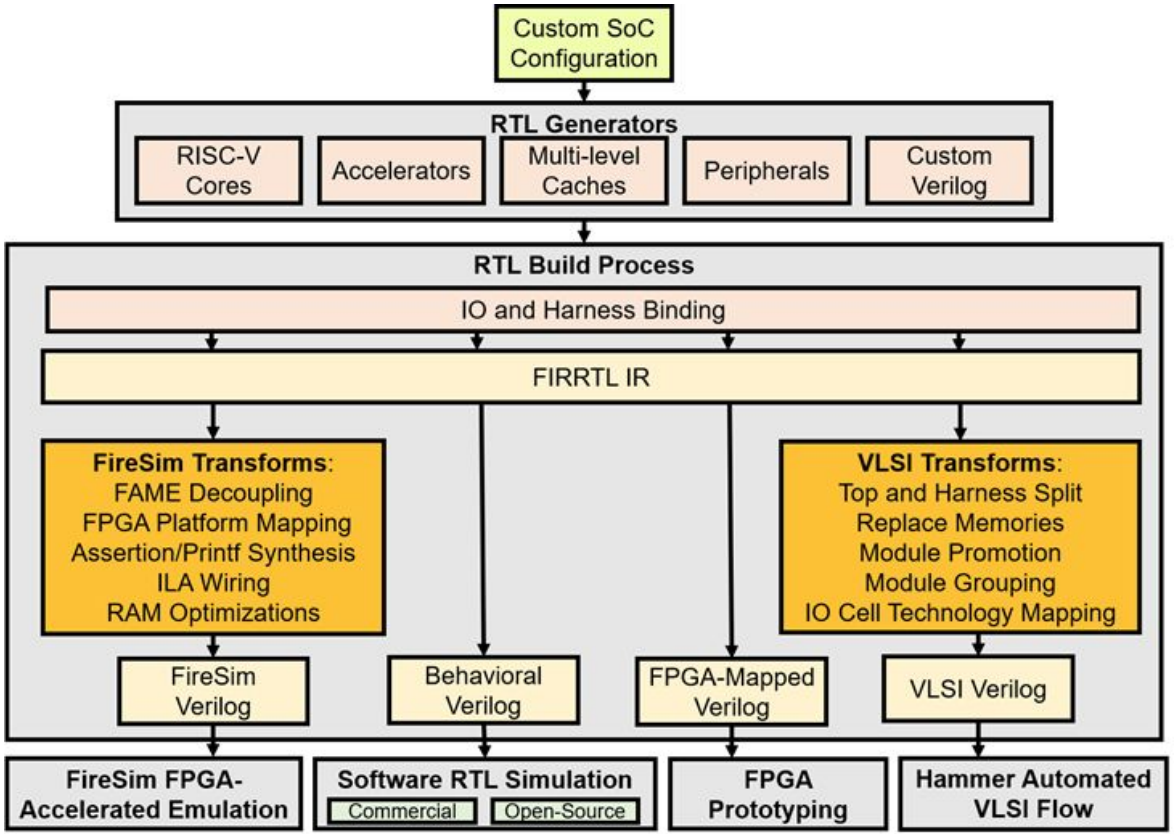
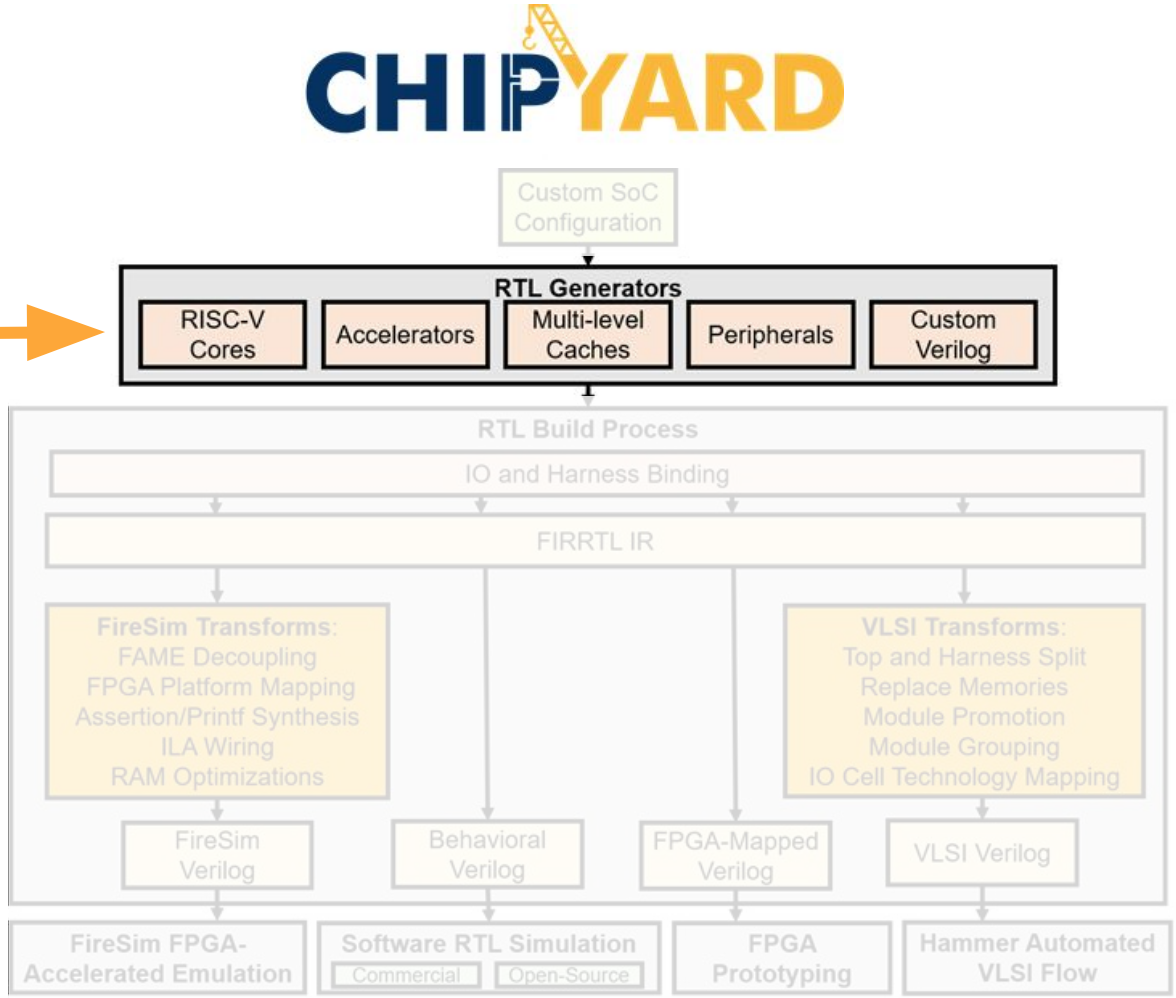
CHIPYARD



https://github.com/ucb-bar/chipyard/ A. Alon, et al., IEEE Micro 2020

Curated Open Source RISC-V IP

Architecture and Generators



https://github.com/ucb-bar/chipyard/ A. Alon, et al., IEEE Micro 2020

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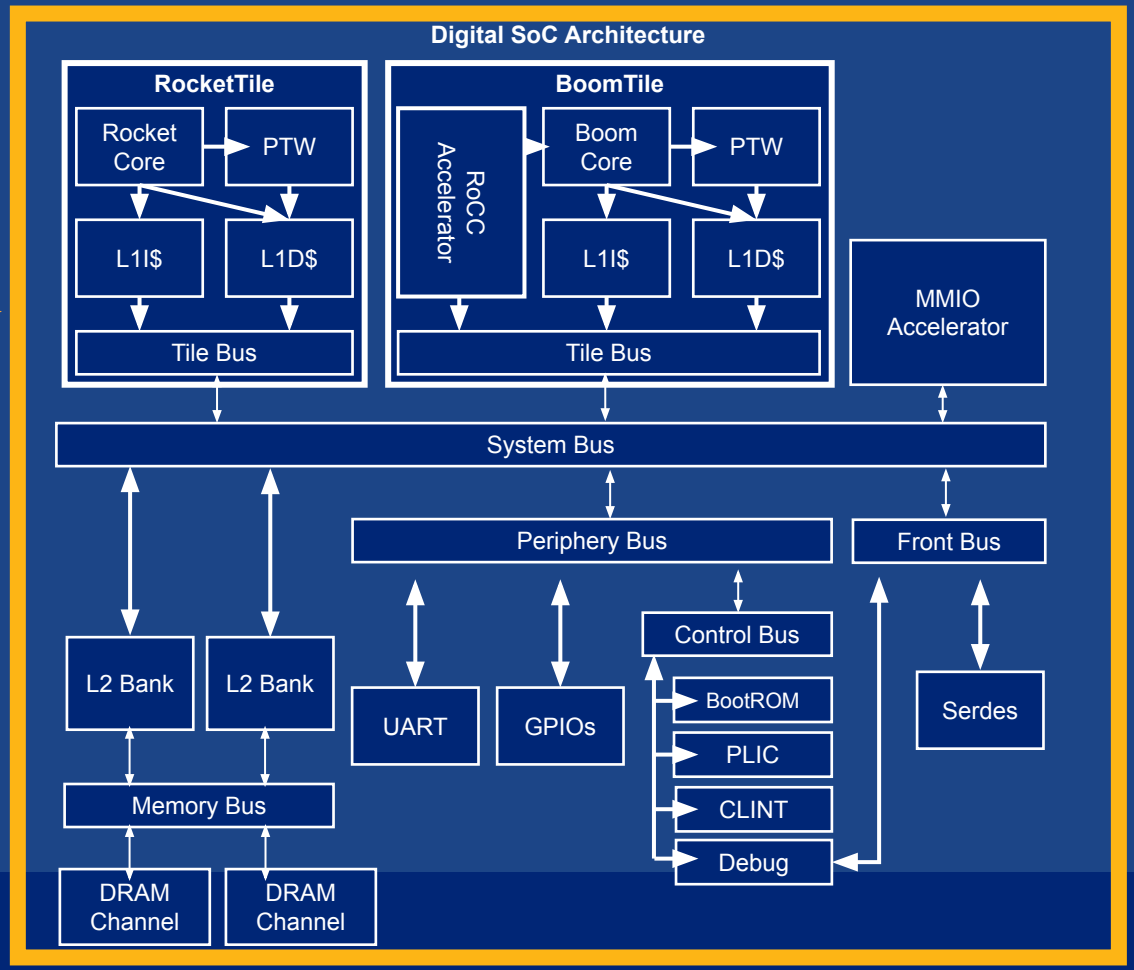
Standard SoC Architecture and Generators



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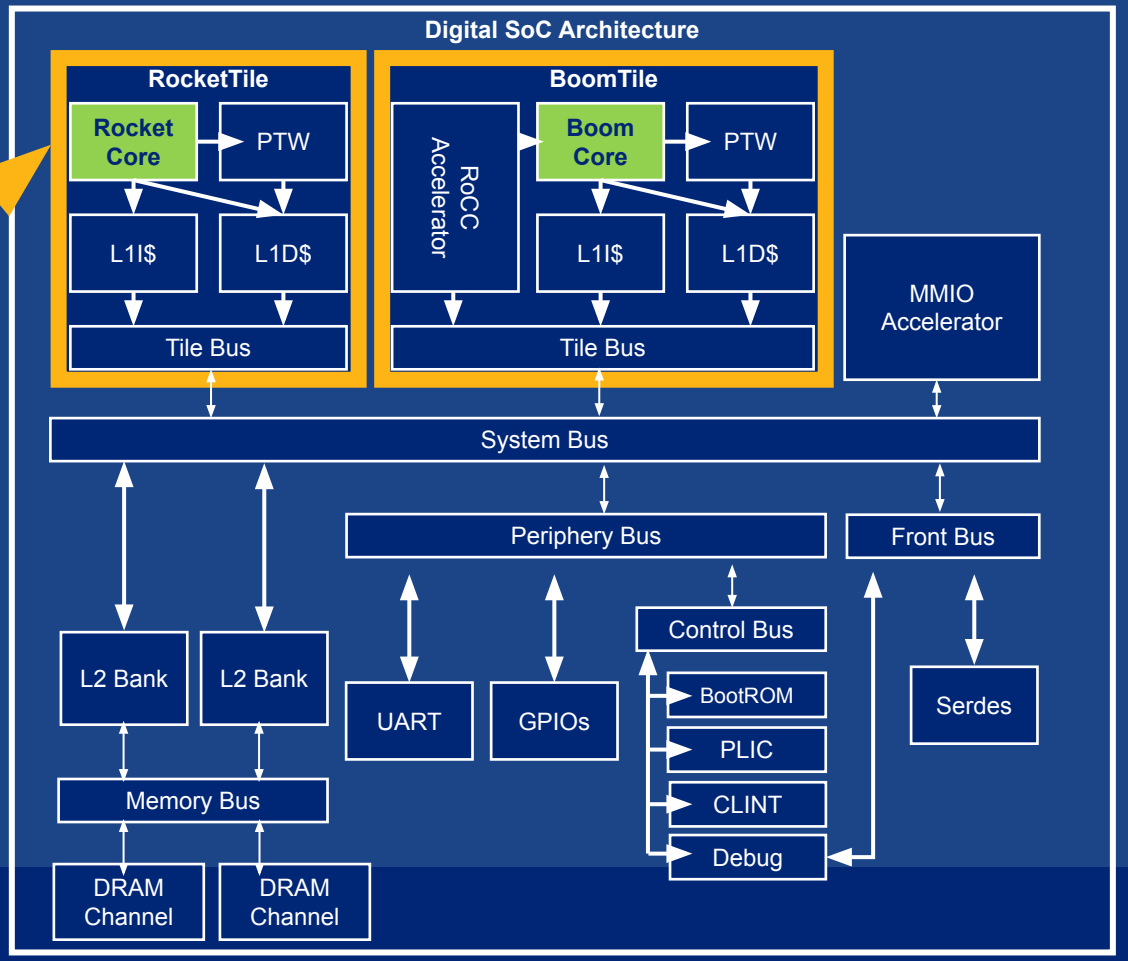
Tiles and Cores

- **Each Tile contains a RISC-V core and private caches**
- Several varieties of cores: Rocket, BOOM, *your own RISC-V core*..



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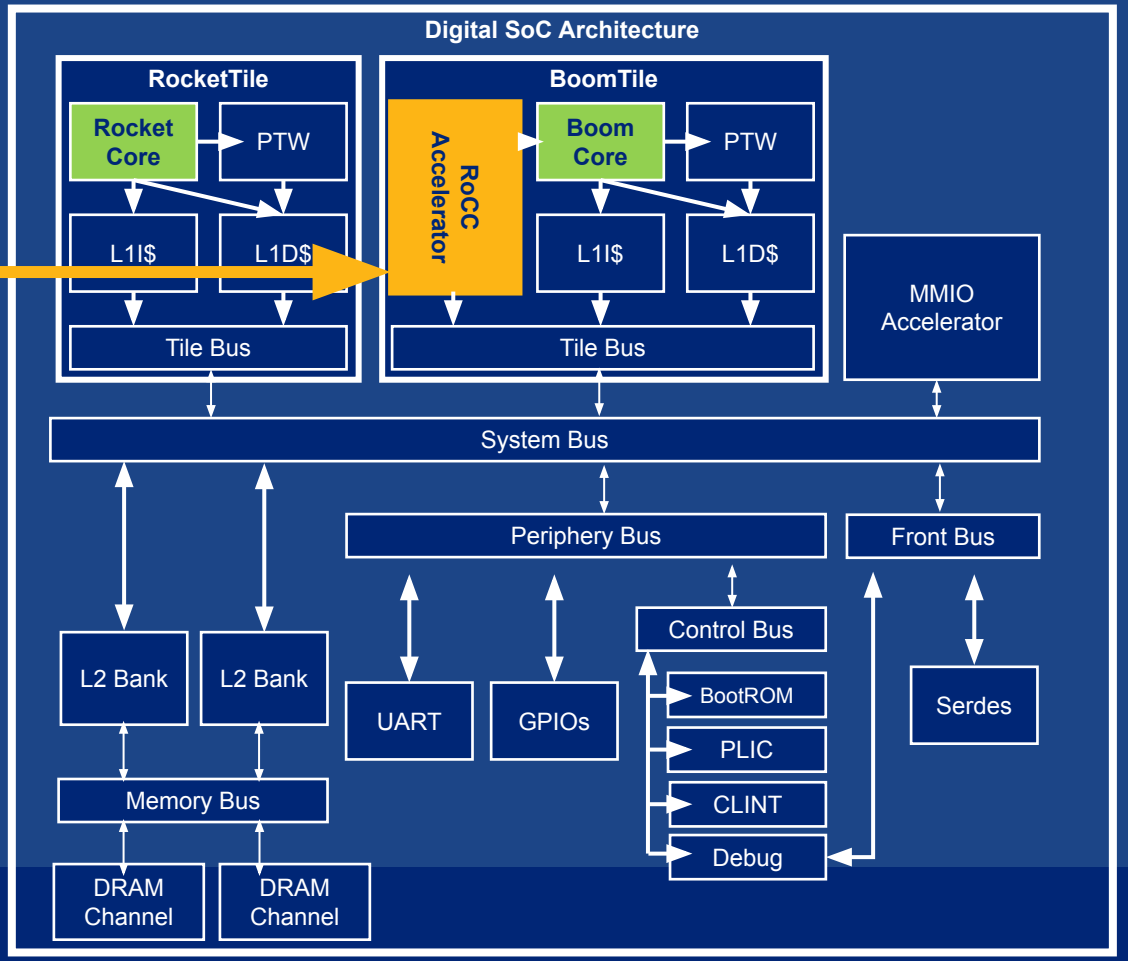
RoCC Accelerators

- **Tightly-coupled accelerator interface**
- Attach custom accelerators to Rocket / BOOM cores



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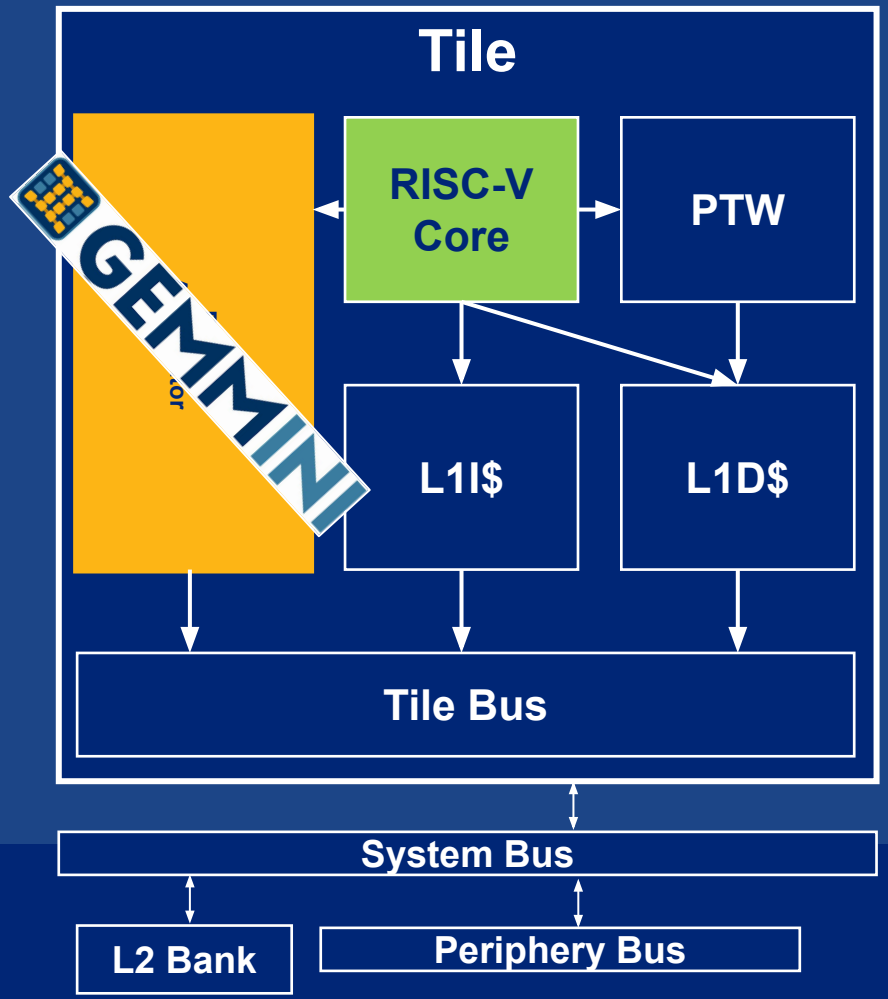
RoCC Accelerators Flexible Interface

Examples:

- **Gemmini ML accelerator**
- Hwacha vector accelerator
- SHA3 accelerator
- *Your own*

https://github.com/ucb-bar/gemmini

H. Genc, et al., DAC 2021



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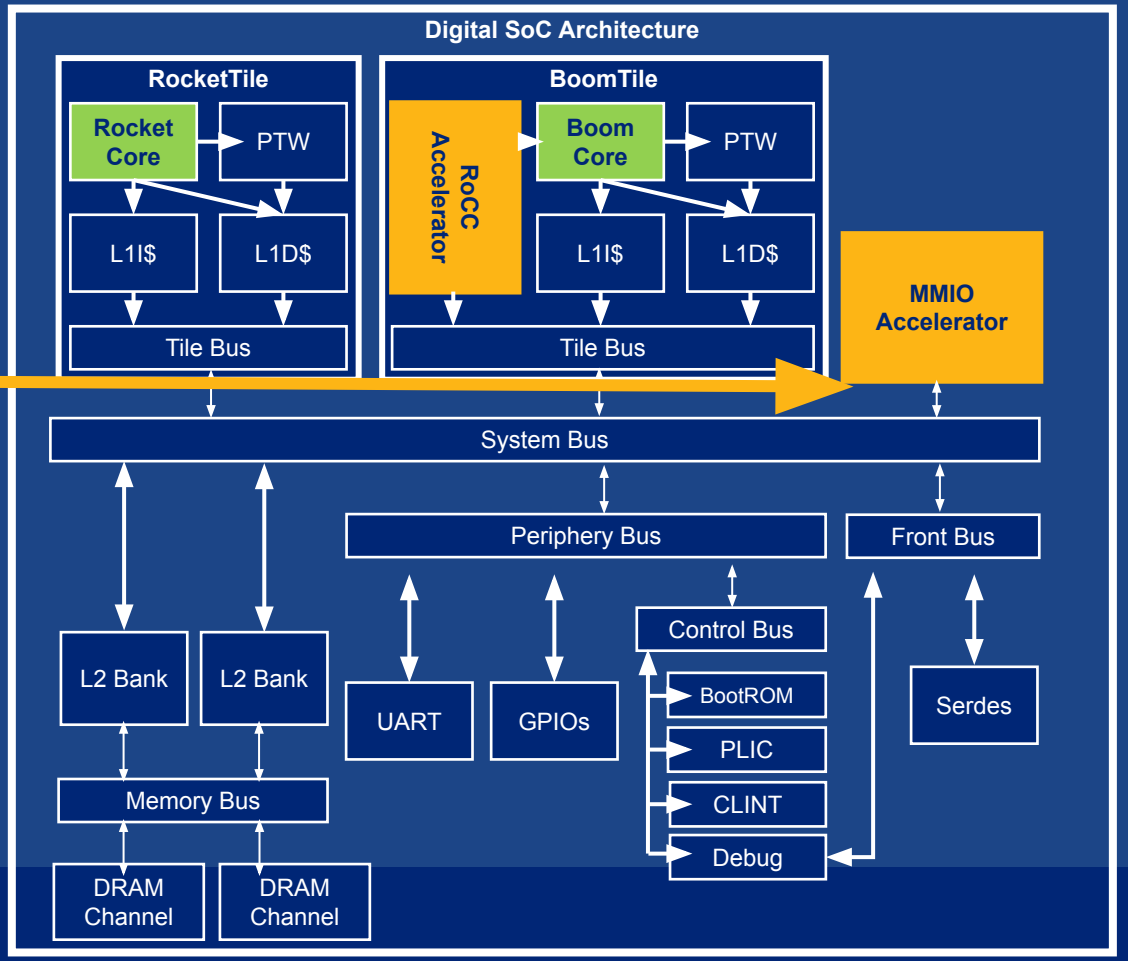
MMIO Accelerators

- **Controlled by MMIO-mapped registers**
- Supports DMA to memory system
- Example: NVDLA.org



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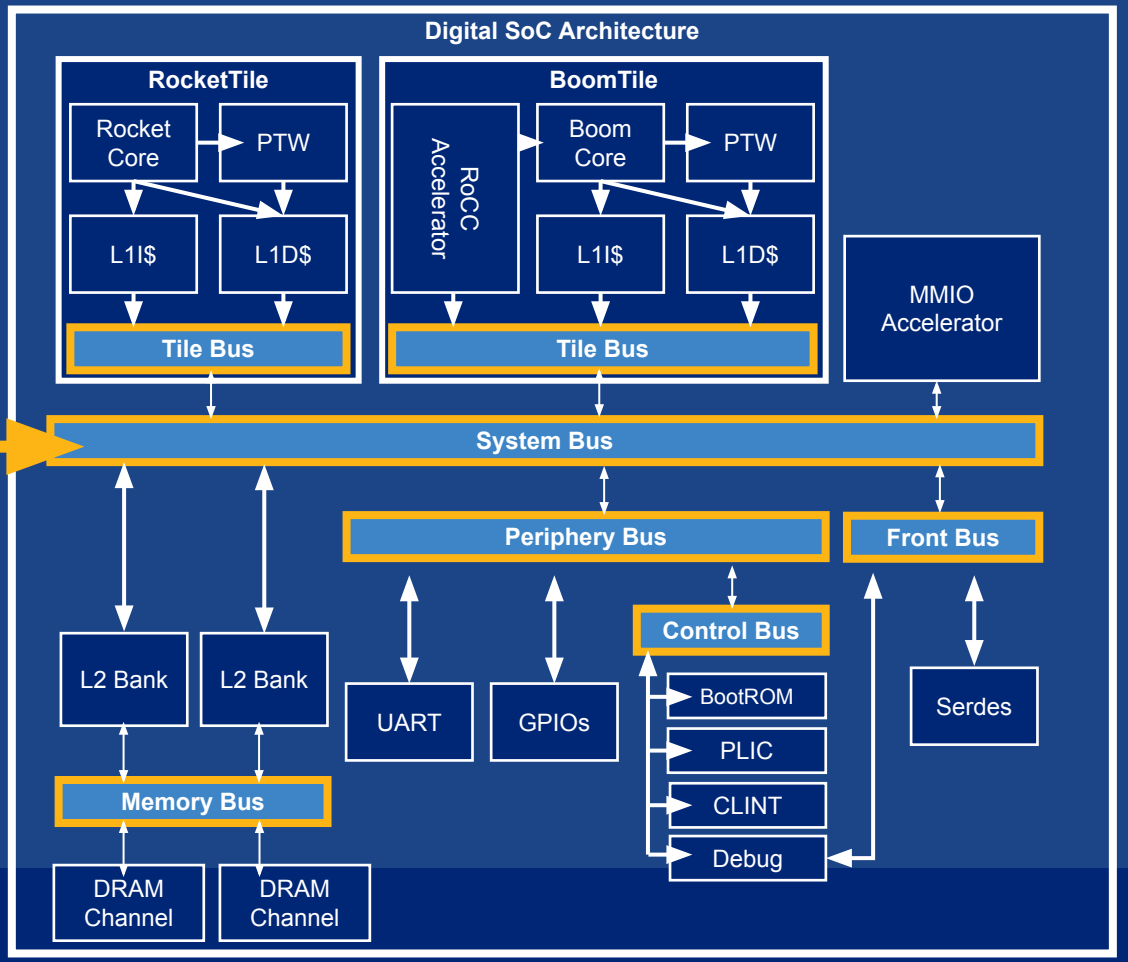
Coherent Interconnect IP

TileLink is an open-source chip scale interconnect standard

- Comparable to AXI/ACE
- Supports accelerators, peripherals, DMA, etc..
- Comes with interconnect IP generator library, adapters



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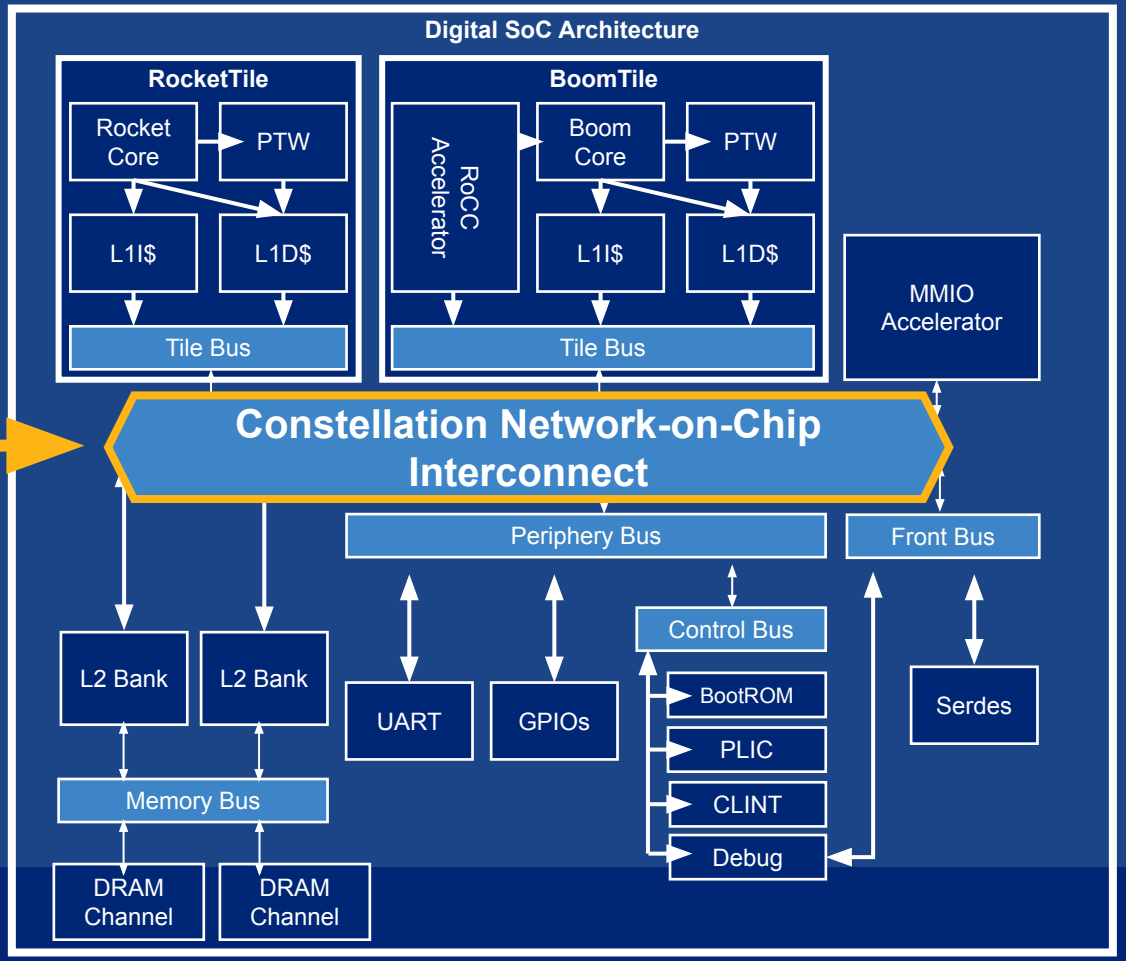
Coherent Interconnect IP

Constellation generates a drop-in NoC replacement for TileLink crossbar buses



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https://github.com/ucb-bar/constellation J. Zhao et al., NoCArc 2022

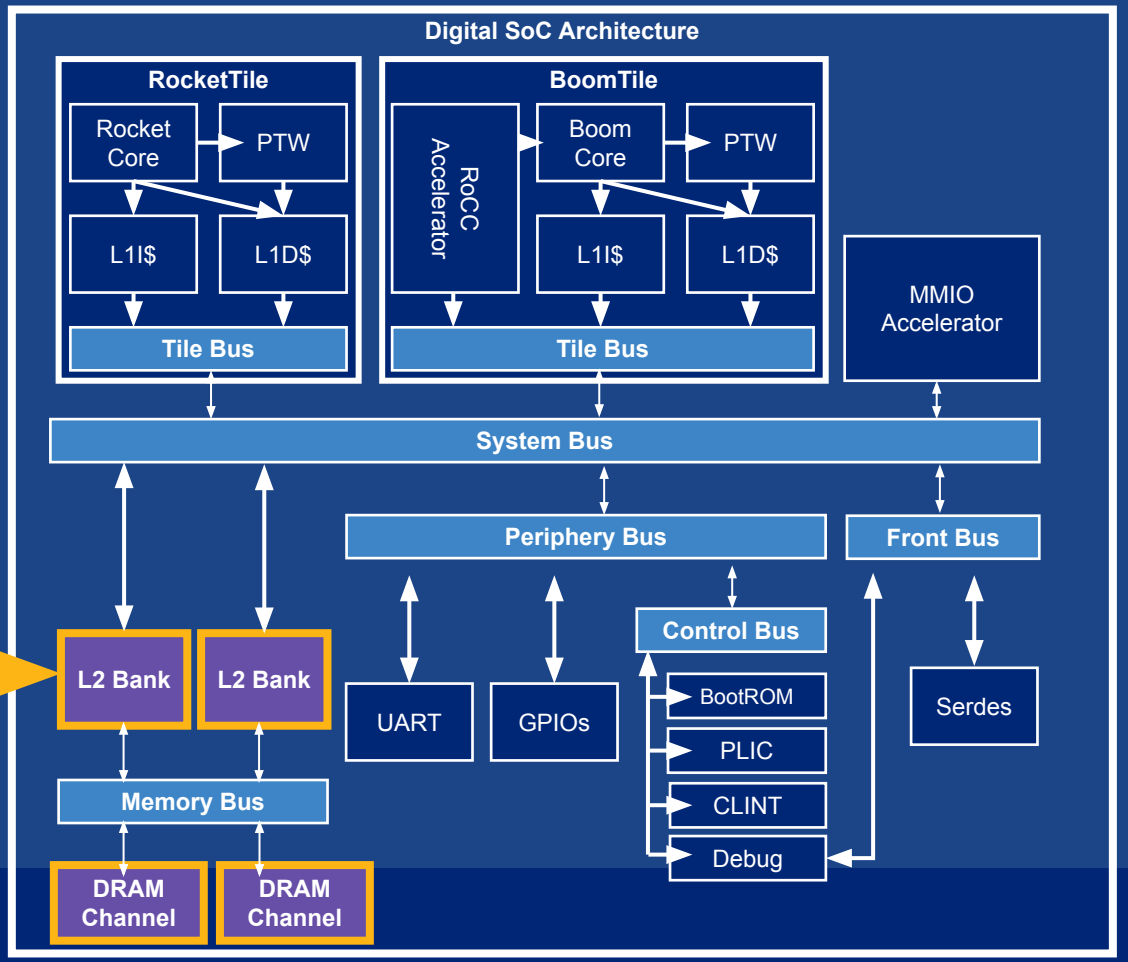
Memory Subsystem

Configurable open source TileLink L2 from SiFive

- Supports broadcast based coherence + incoherent systems

AXI-4 interface ports to external DRAM memory controller

- *or LPDDR4X controller + PHY (WIP)*



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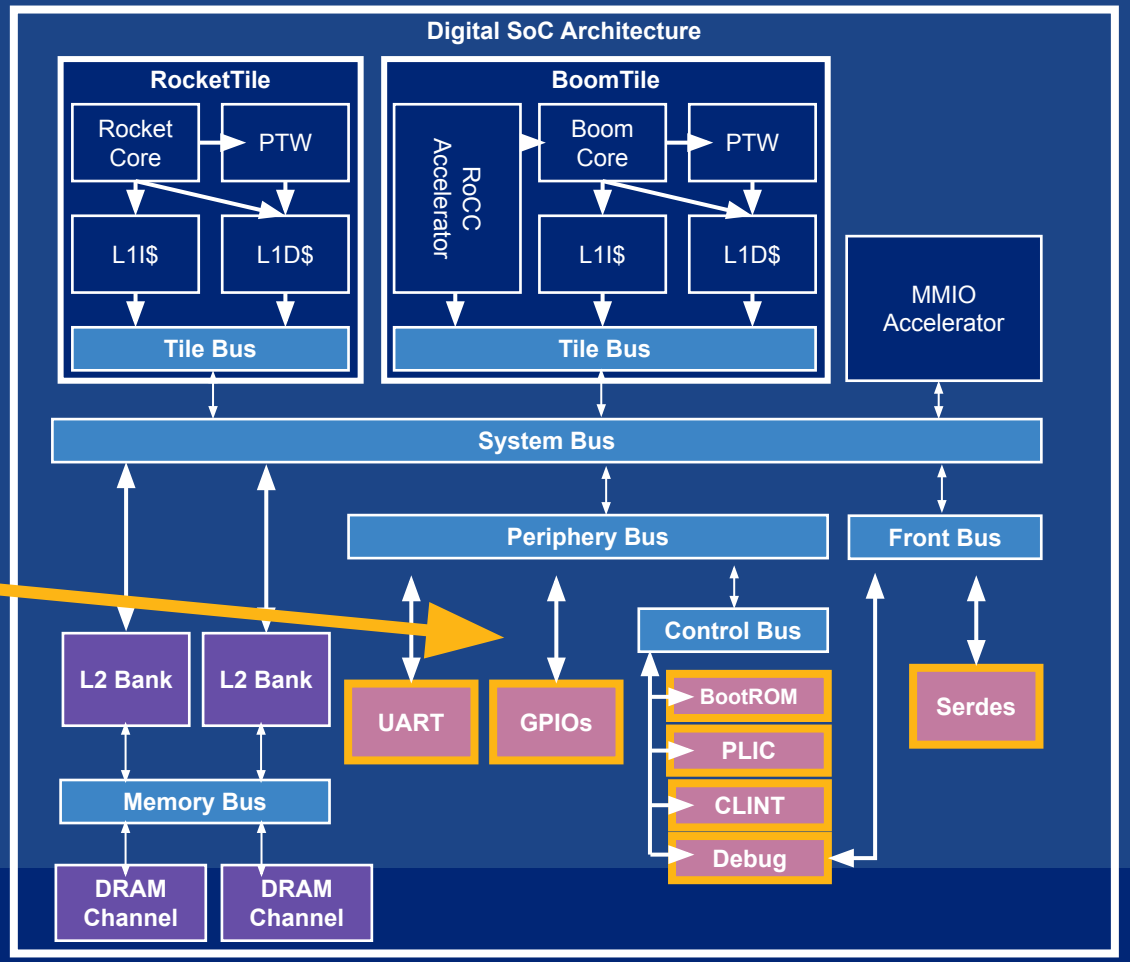
Peripherals, IO, Test Chip IP…

Basic essentials, all free and open source

- Interrupt controllers
- JTAG, debug module
- BootROM
- UART, GPIOs, SPI, I2C, PWM..
- Clock-management devices
- SerDes
- Scratchpads
- *UCIe (WIP)*



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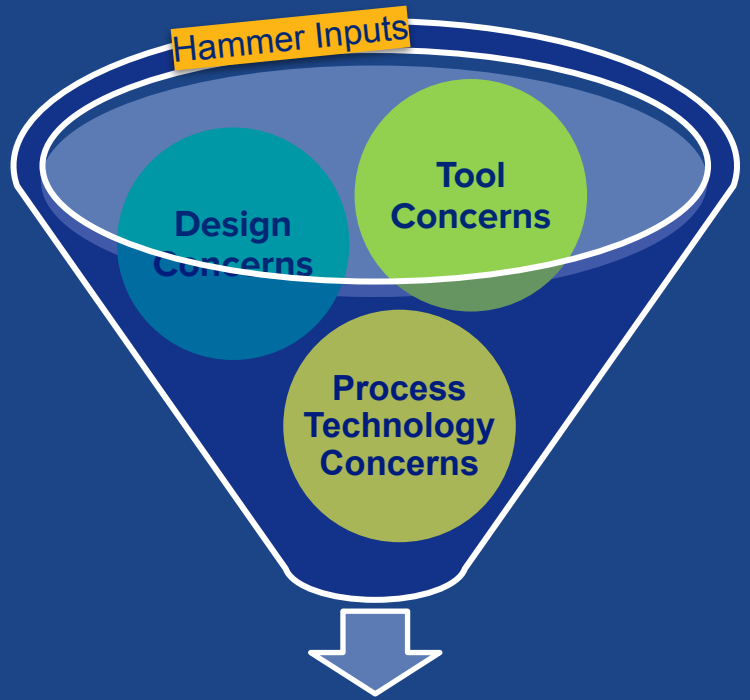
Hammer VLSI Makes the SoCs Manufacturable

Hammer is a modular VLSI flow & API enabling **reusability + tool abstraction**.

Works with **open source**:
SkyWater, OpenRoad..

Works with **commercial**:
Intel, TSMC, Cadence, Synopsys..

Works for our classes!



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https://github.com/ucb-bar/hammer H. Liew et al., DAC 2021

The Tapeout Sprint

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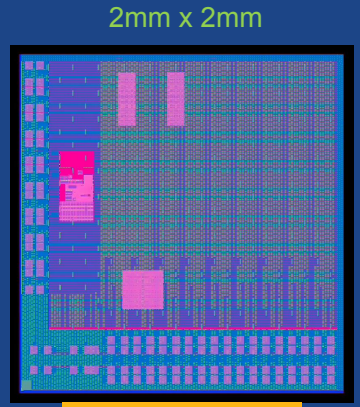
A Minimal-Prerequisite Infrastructure Crash Course

Class labs enable getting to a bare-bone SoC in 5 weeks.

Lab 1	Lab 2	Lab 3	Lab 4	Lab 5
Intro to Chipyard	**Physical Design With Hammer**	**Custom Block Design**	**Characterizing Custom Blocks**	**SoC Integration**
Generate starting RTL for the SoC	*Synthesize, PnR, and DRC the starter RTL*	*Create a custom AMS inverter block*	*Create front end views for the custom macro*	*Place starter RTL into a preconfigured chip frame*

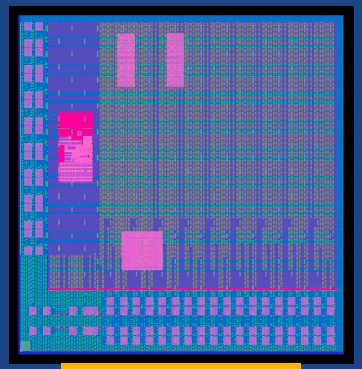


Starter Design

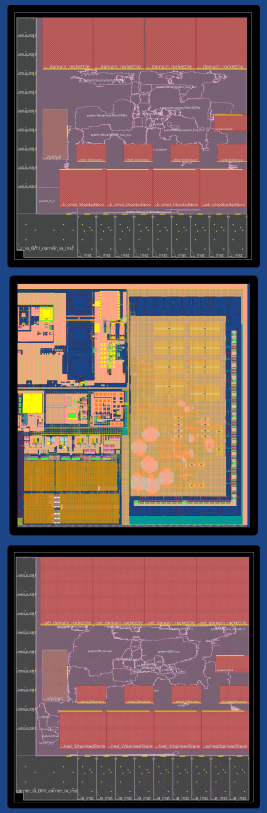
(+ additional analog labs exist)

From Lab 5 Starter SoC To Rapid Creativity

RISC-V Rocket core
Memory (L2$ ..)
Peripherals (JTAG ..)
Ring PLL
Intel pad drame
A lot of empty ..



Starter Design



Additional cores

Design extensions

Tightly coupled co-processors

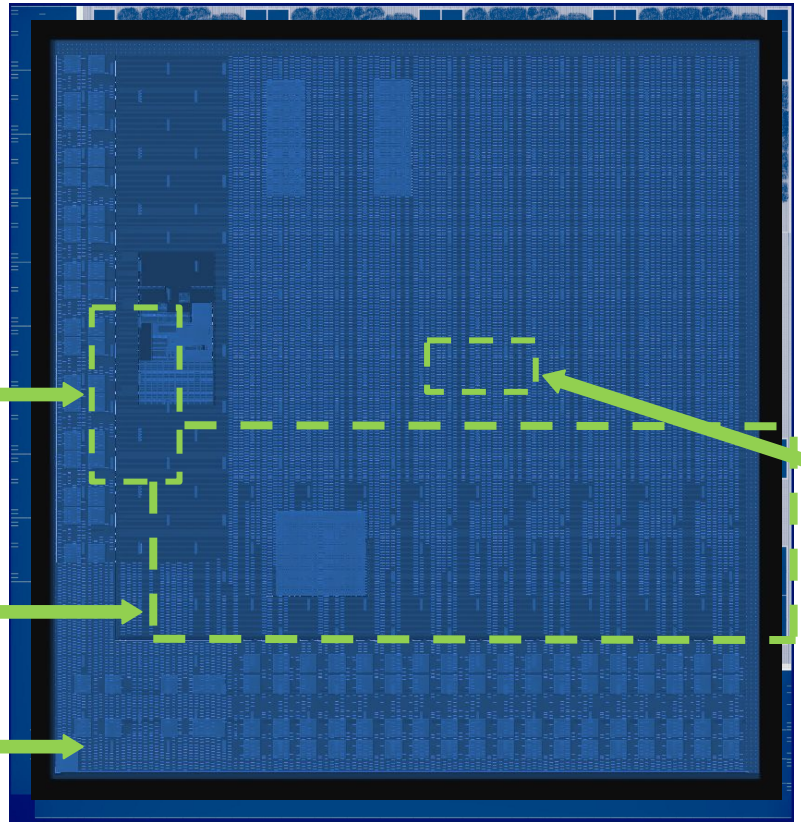
MMIO accelerators

Mixed signal designs

Research validation
New ecosystem IP
IP improvements

The Making of an SoC for Smart Audio: COSMIC

Starter Design



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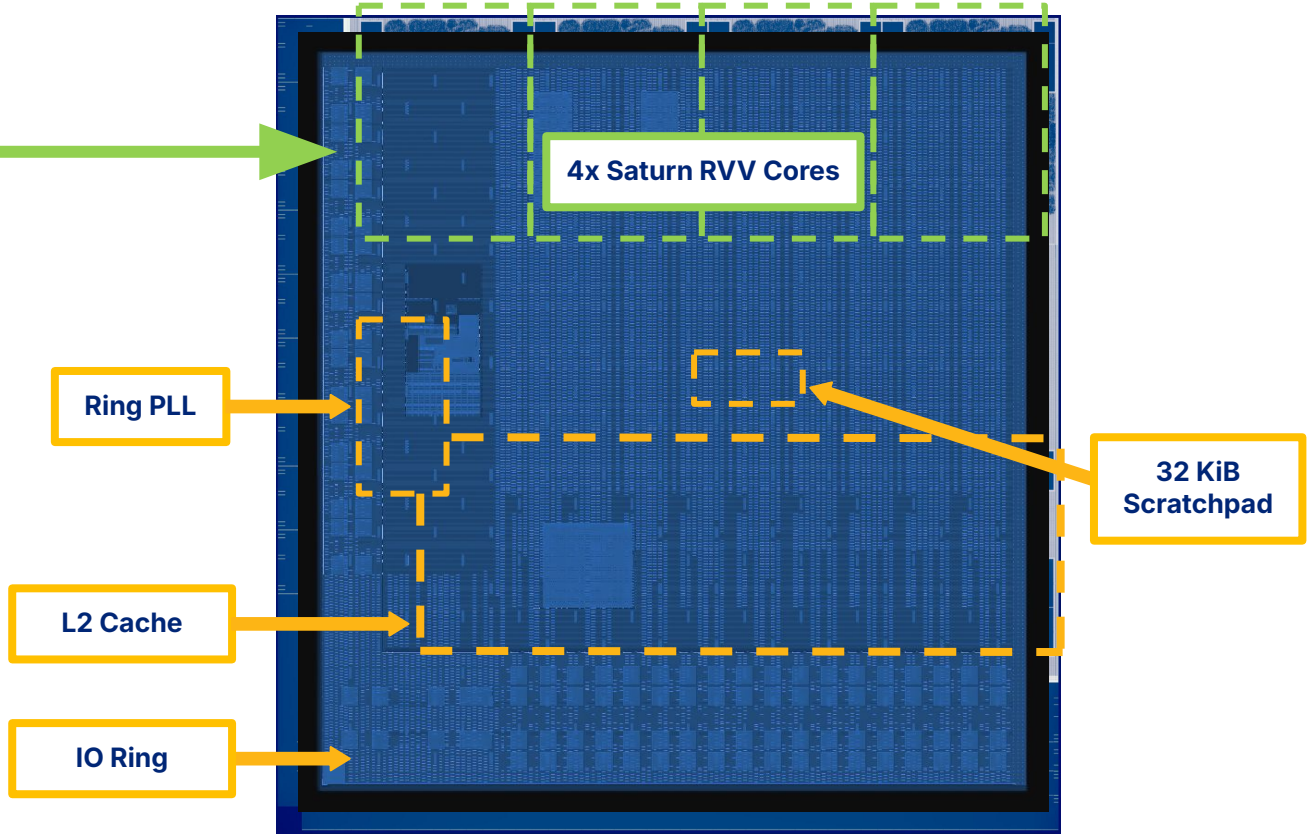
The Making of an SoC for Smart Audio: COSMIC

New **Saturn-V RV64GC** cores with RVV1.0 vector units

256-bit vector length, 64-bit datapath width



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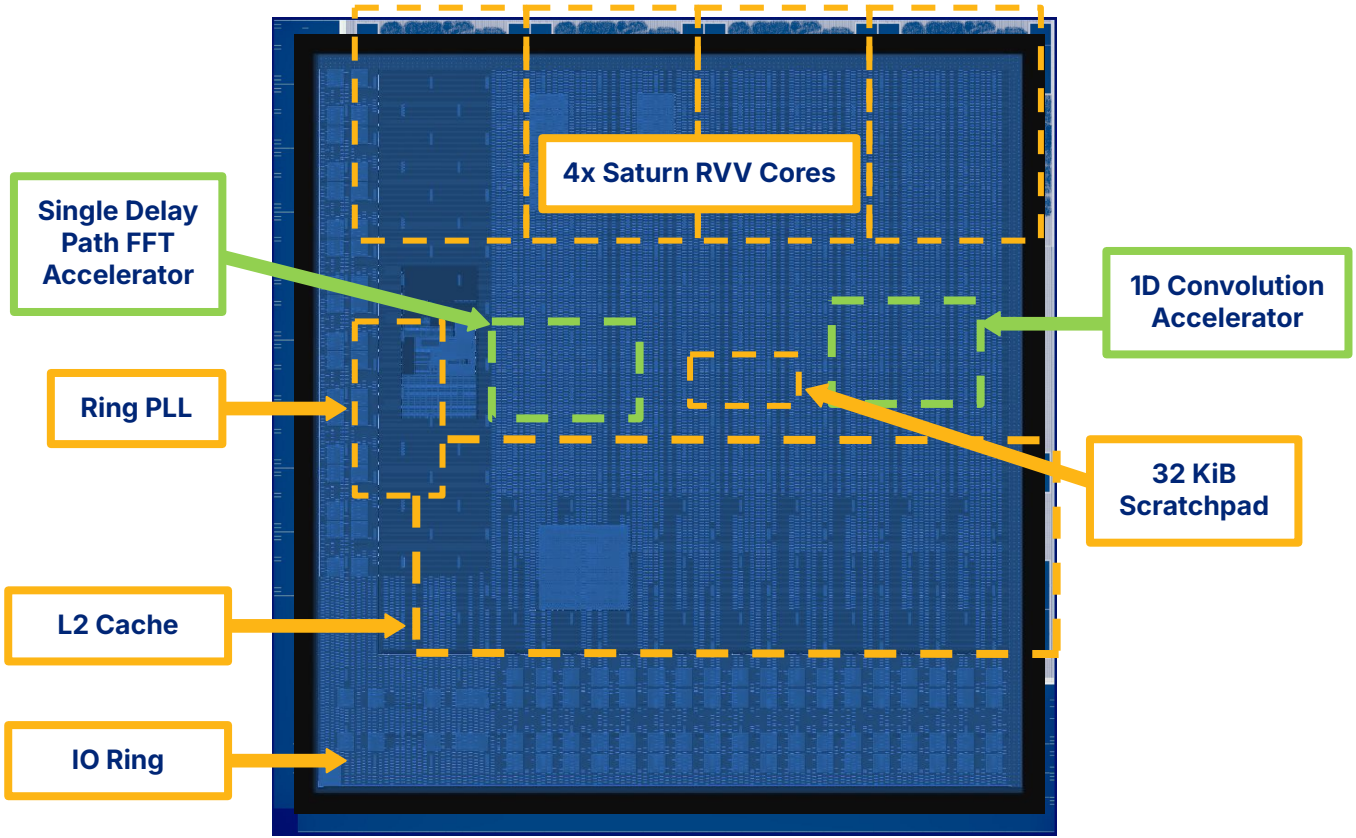
https://github.com/ucb-bar/saturn-vectors J. Zhao et al.

The Making of an SoC for Smart Audio: COSMIC

1D Convolution Accelerator

SDF-FFT Accelerator
MMIO 128-point radix-2 pipelined implementation



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https://github.com/milovanovic/sdf-fft V. Milovanović et al., MIEL 2019

The Making of an SoC for Smart Audio: COSMIC

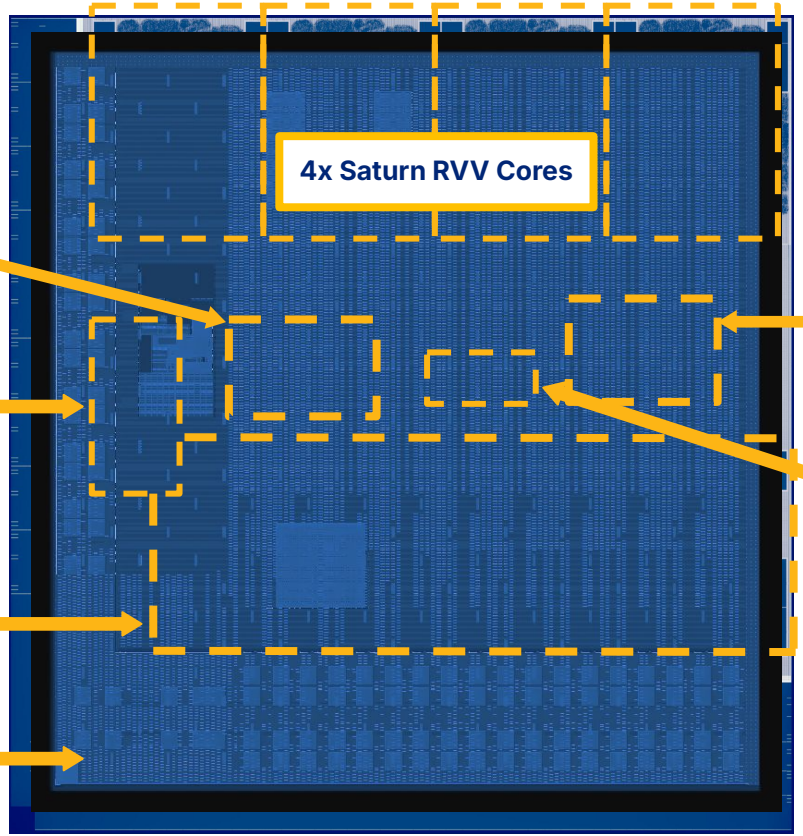
DMA Engine

fully programmable
7 indep channels

Audio Interface

4x I²S stereo channels with full DMA support

2x integrated 16-bit ΣΔ DACs for analog audio output



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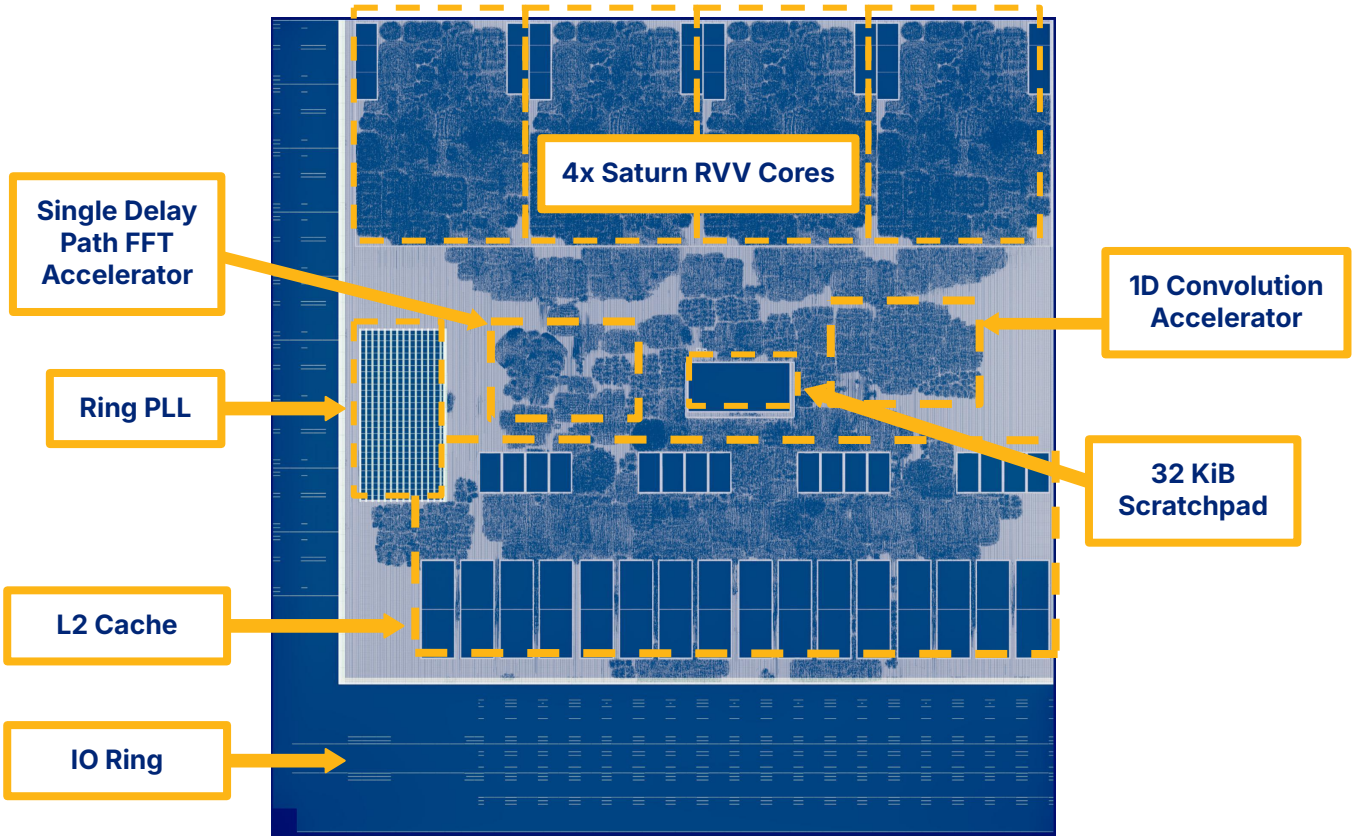
The Making of an SoC for Smart Audio: COSMIC

Result: COSMIC

RISC-V-based SoC optimized for energy efficient audio DSP and ML workloads

Intel 16nm FinFET

2mm x 2mm die



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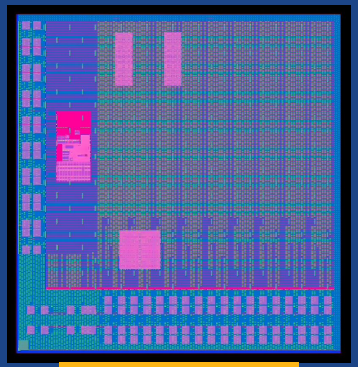
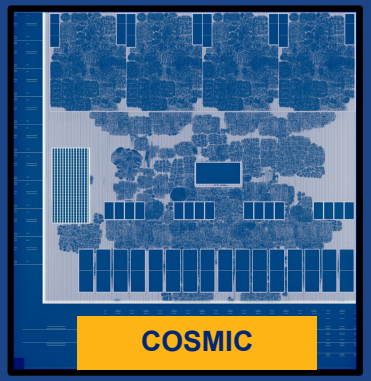
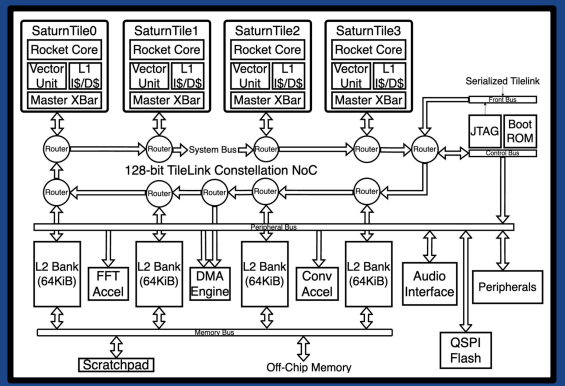
Will be presented by E. Gao et al., at ESSERC 2025

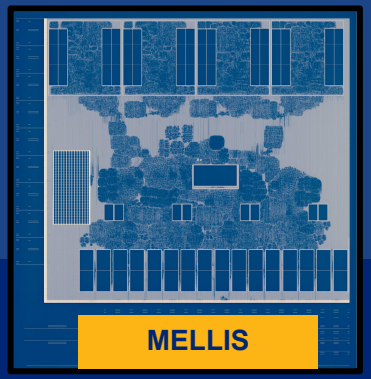
COSMIC's Close Sibling MELLIS for ML

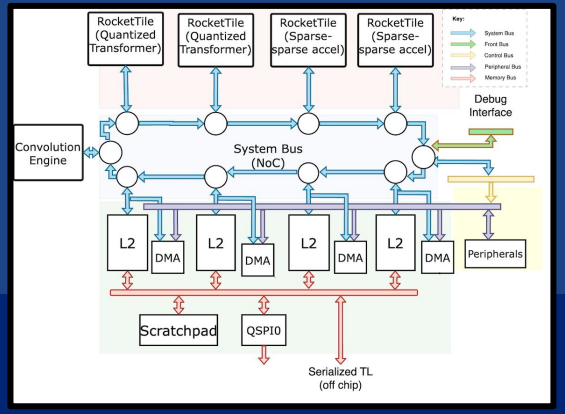


Starter Design









Similarities:

- 128b TileLink NoC
- Intel Ring PLL
- Intel IO slice ring
- Bus hierarchy
- 4× 64 KiB L2$
- JTAG, QSPI boot..

One integration team, one flow = success % up

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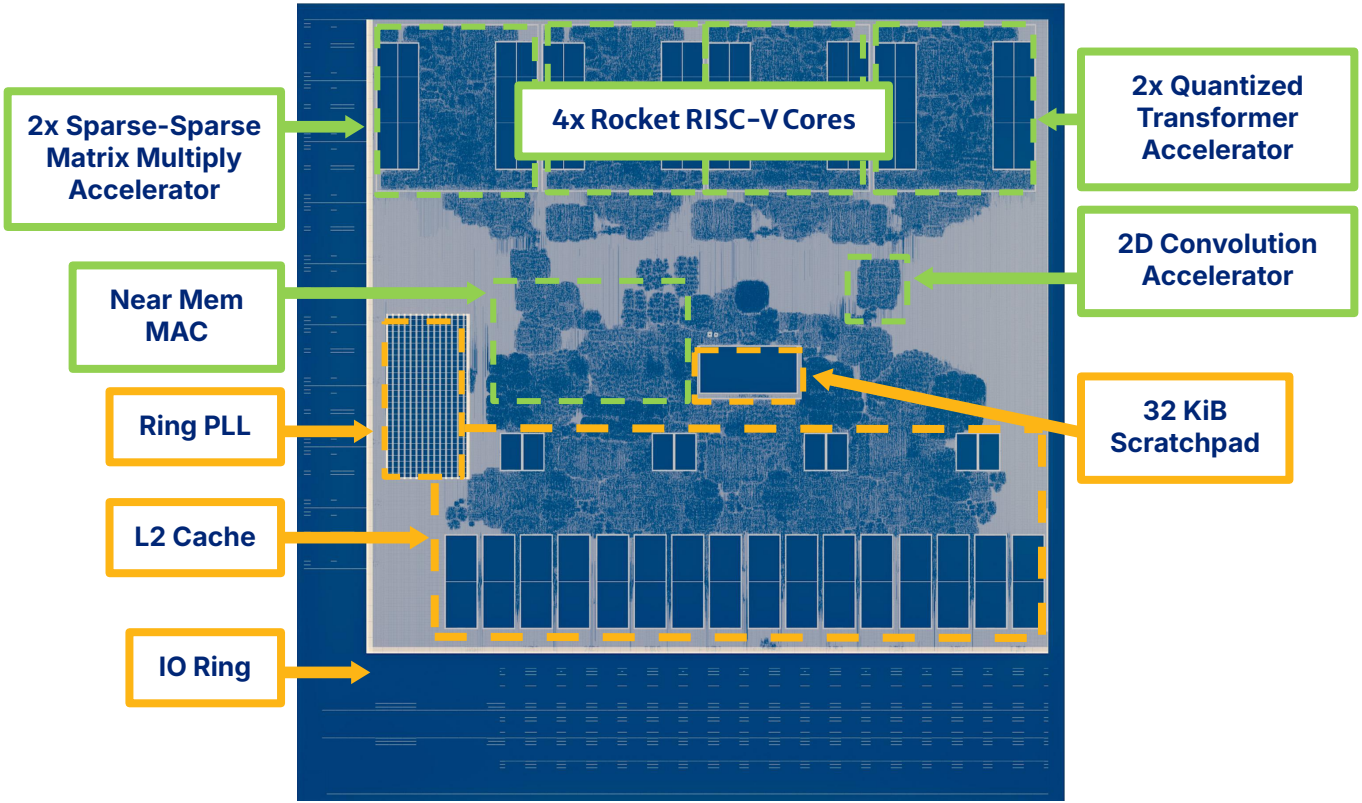
MELLIS Architecture All In On Edge ML

Result: tightly coupled & near memory ML acceleration

Enables fusing GCNs with CNNs, such as in satellite imagery classification.



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See MELLIS predecessor NeCTAr, HotChips 2024

What about AMS? RF?

Can **programmatic hardware generation** and **schematic-driven analog design** coexist?

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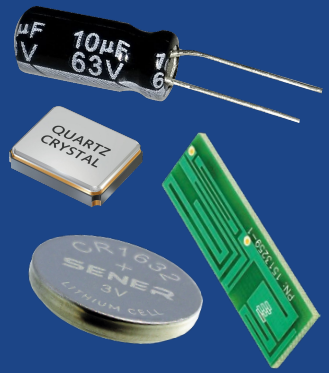
Beyond Digital Workloads: SCµM-V Micromote SoC

IoT, microbots, agriculture, biomedical.. require a **wireless sensor node.**

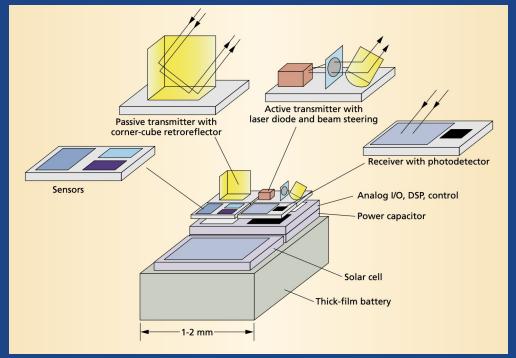
On chip integration enables 10x* reduction in size, weight, cost, power:

2.4GHz with no PCB, external passives, PLLs, or external Xtal ref.

DA14530 Dialog Semi

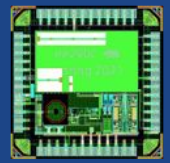


cm-scale



mm-scale

"Smart Dust [...]"
B. Warneke et al., Computer 2001



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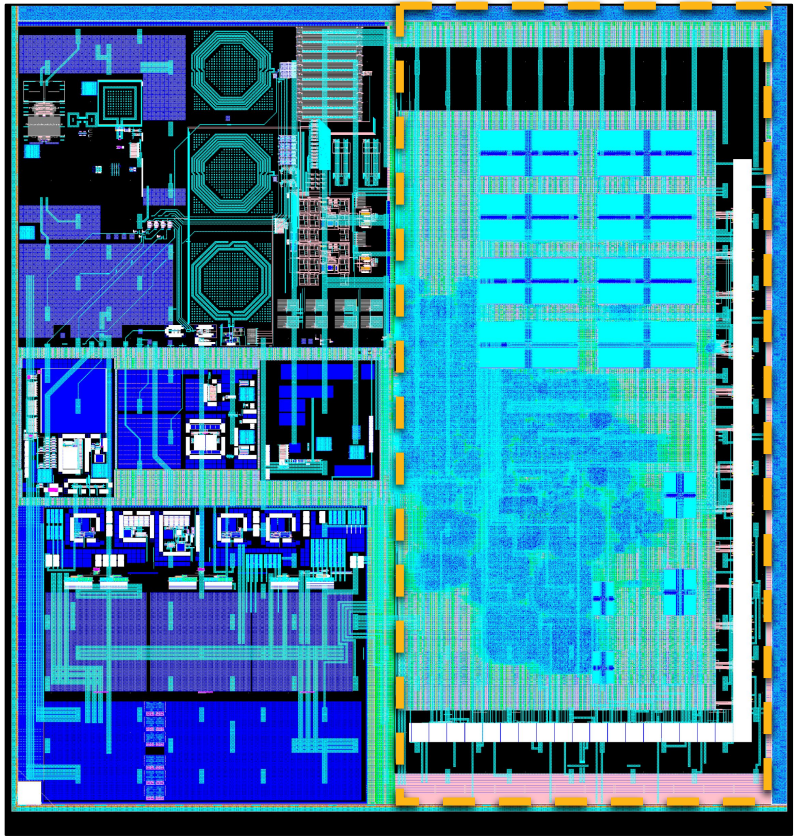
*vs cm-scale systems

SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip

Agile Integration

Using Hammer flexibility to efficiently PnR using a hierarchy of digital Chip Tops including the Chipyard digital core as a hardened macro.

D. Lovell et al., WOVEN 2025



Chipyard Digital Core

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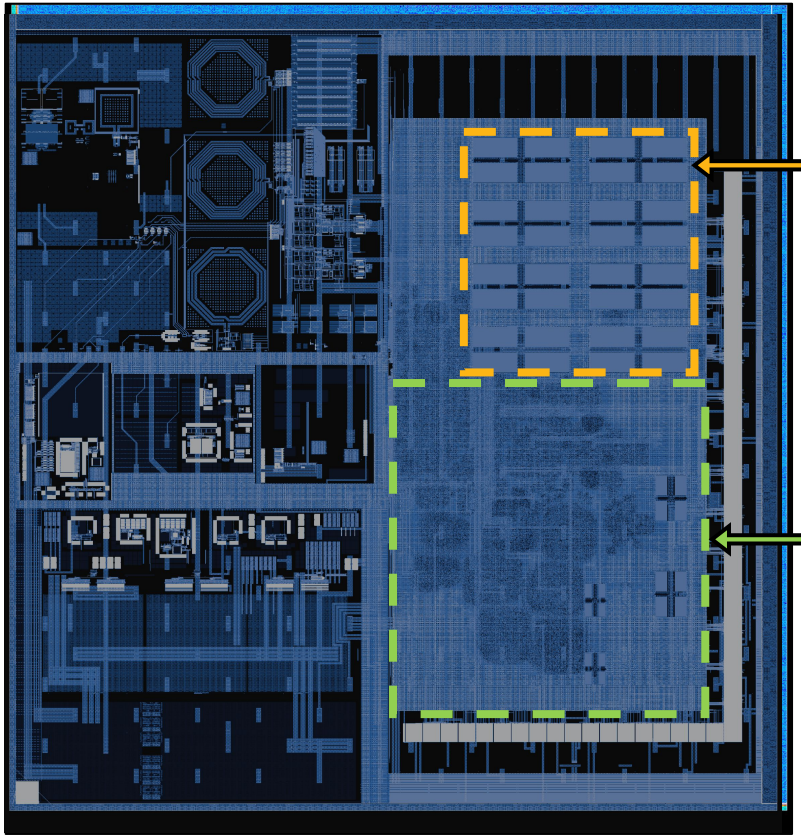
SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip



256 kB SRAM

Cryptography Acceleration

RISC-V 32b Core, BLE & IEEE 802.15.4 modem, AES/SHA-256/ECC accelerators

See predecessor SCµM-V23 IEEE CrystalFreeIoT Workshop 2024

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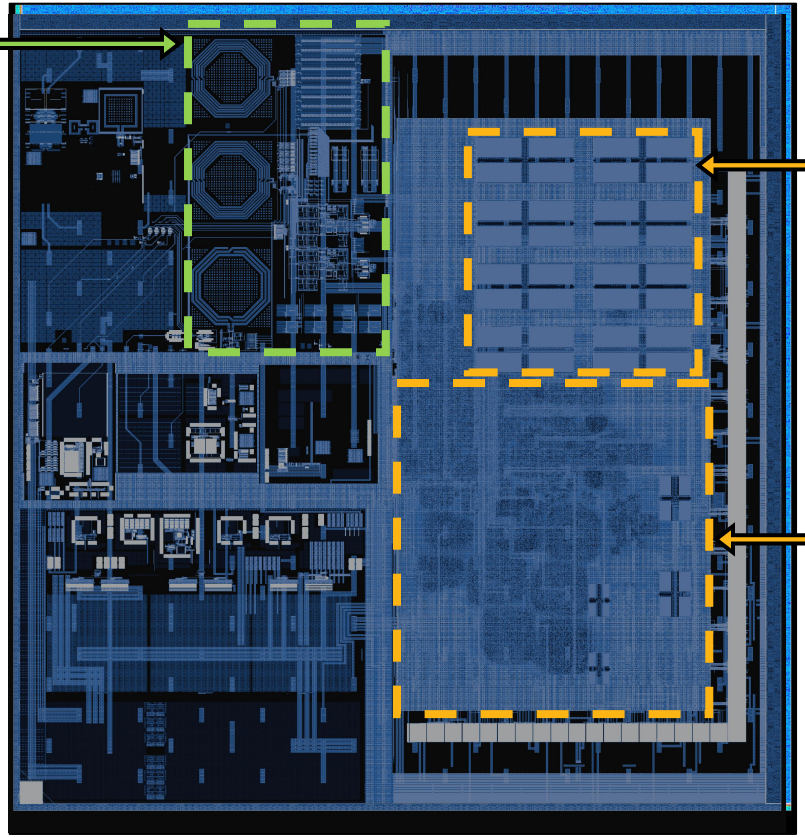
SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip

2.4 GHz BLE &
IEEE 802.15.4 Transceiver

Low Power
RF Design



256 kB
SRAM

Cryptography
Acceleration

RISC-V 32b Core,
BLE & IEEE
802.15.4 modem,
AES/SHA-256/E
CC accelerators

See predecessor
SCµM-V23 IEEE
CrystalFreeIoT
Workshop 2024

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SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip

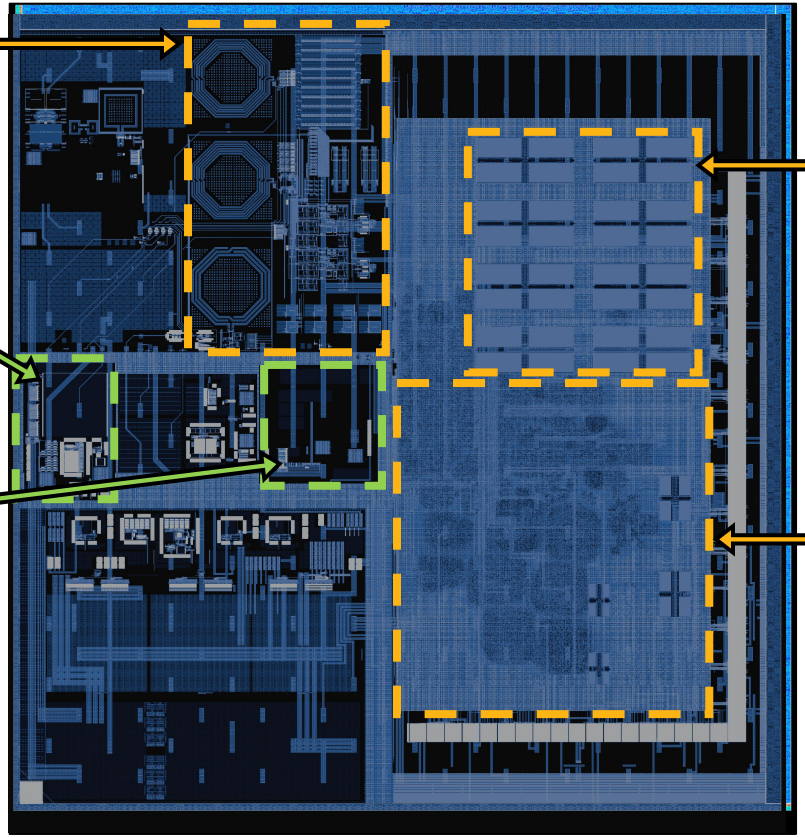
2.4 GHz BLE &
IEEE 802.15.4 Transceiver

Low Power
RF Design

Interface Multiple
Sensor Types

General-Purpose
Analog Front-End

µV-Precision ADC



256 kB
SRAM

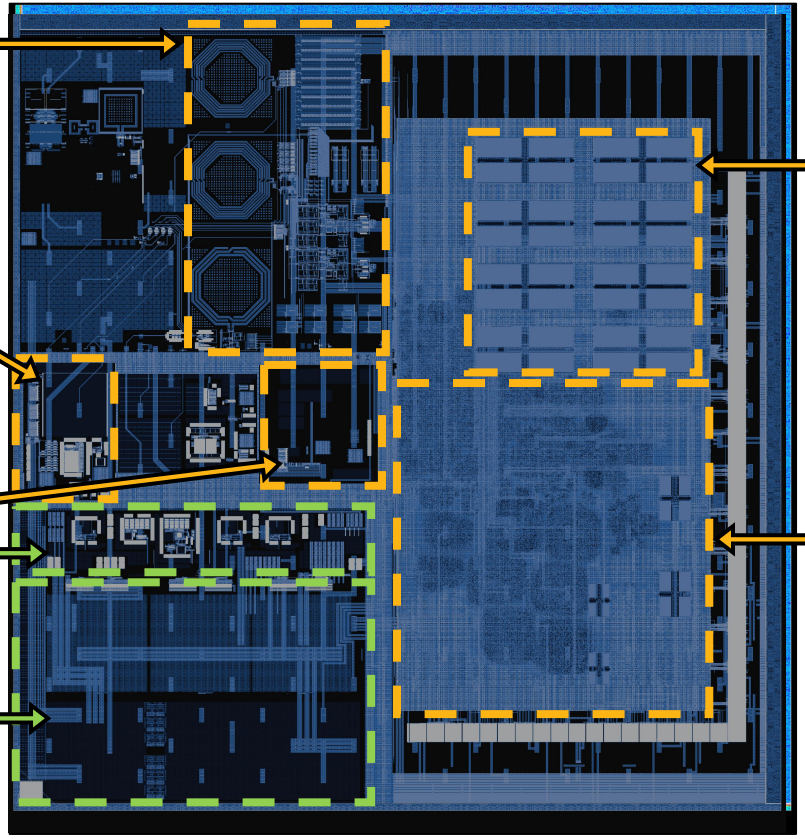
Cryptography
Acceleration

RISC-V 32b Core,
BLE & IEEE
802.15.4 modem,
AES/SHA-256/E
CC accelerators

See predecessor
SCµM-V23 IEEE
CrystalFreeIoT
Workshop 2024

UC Berkeley

SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip



2.4 GHz BLE & IEEE 802.15.4 Transceiver

Low Power RF Design

Interface Multiple Sensor Types

General-Purpose Analog Front-End

µV-Precision ADC

LDOs, Bandgap Voltage Reference, and Current Reference

DC-DC Converter

On Chip Power Management

256 kB SRAM

Cryptography Acceleration

RISC-V 32b Core, BLE & IEEE 802.15.4 modem, AES/SHA-256/ECC accelerators

UC Berkeley

See predecessor SCµM-V23 IEEE CrystalFreeIoT Workshop 2024

SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip

2.4 GHz BLE & IEEE 802.15.4 Transceiver

Low Power RF Design

Interface Multiple Sensor Types

On Chip Crystal Free Clock

General-Purpose Analog Front-End

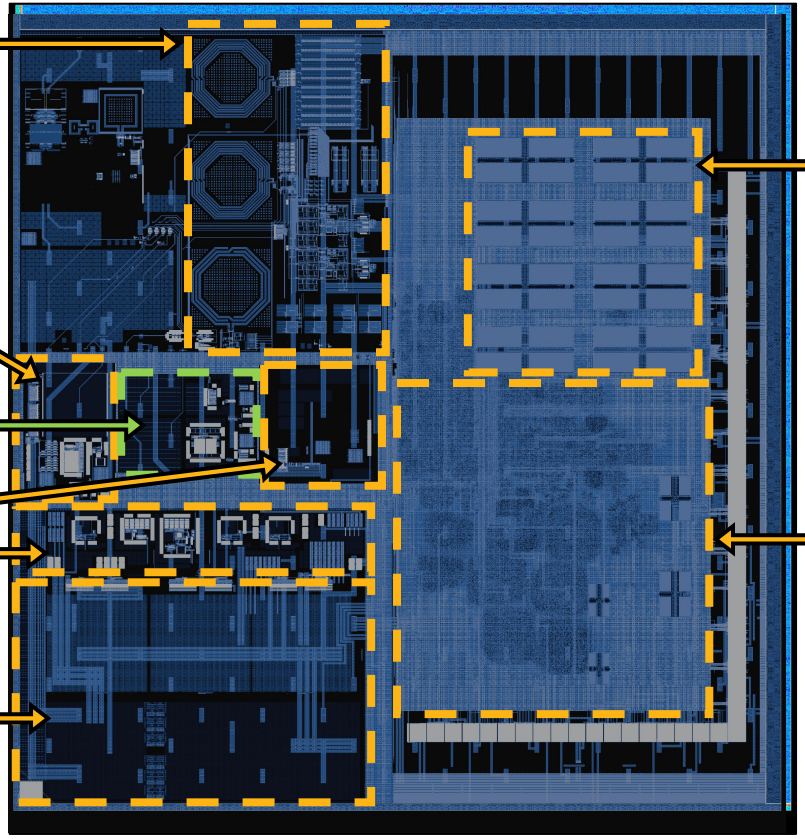
Clock Generation

µV-Precision ADC

LDOs, Bandgap Voltage Reference, and Current Reference

DC-DC Converter

On Chip Power Management



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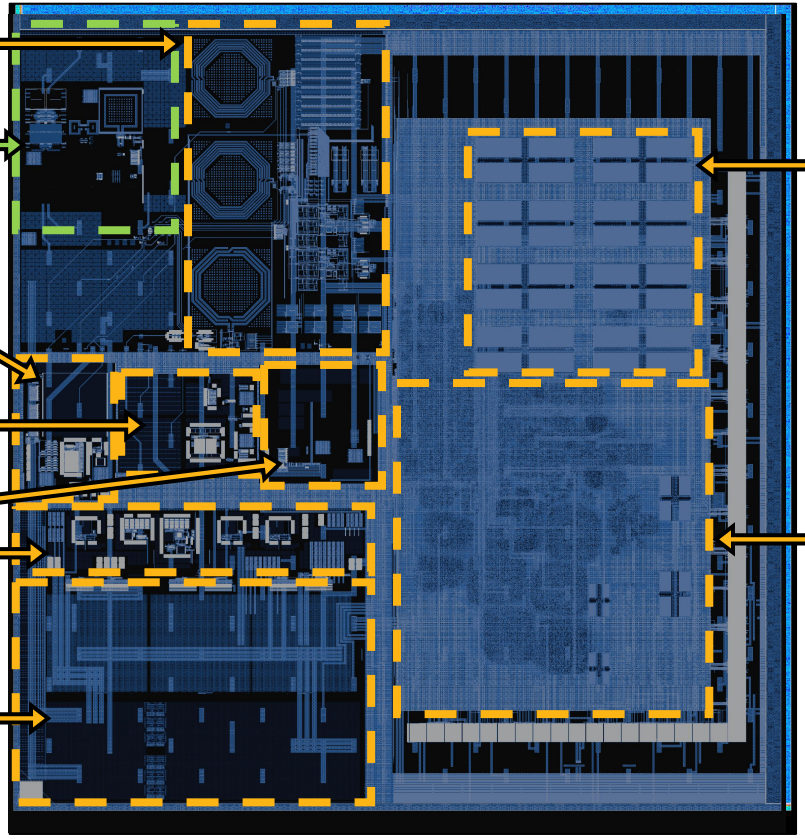

2.4 GHz BLE & IEEE 802.15.4 Transceiver

Low Power RF Design

90 GHz FMCW Radar

Interface Multiple Sensor Types

General-Purpose Analog Front-End

On Chip Crystal Free Clock

Clock Generation

µV-Precision ADC

LDOs, Bandgap Voltage Reference, and Current Reference

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See predecessor SCµM-V23 IEEE CrystalFreeIoT Workshop 2024

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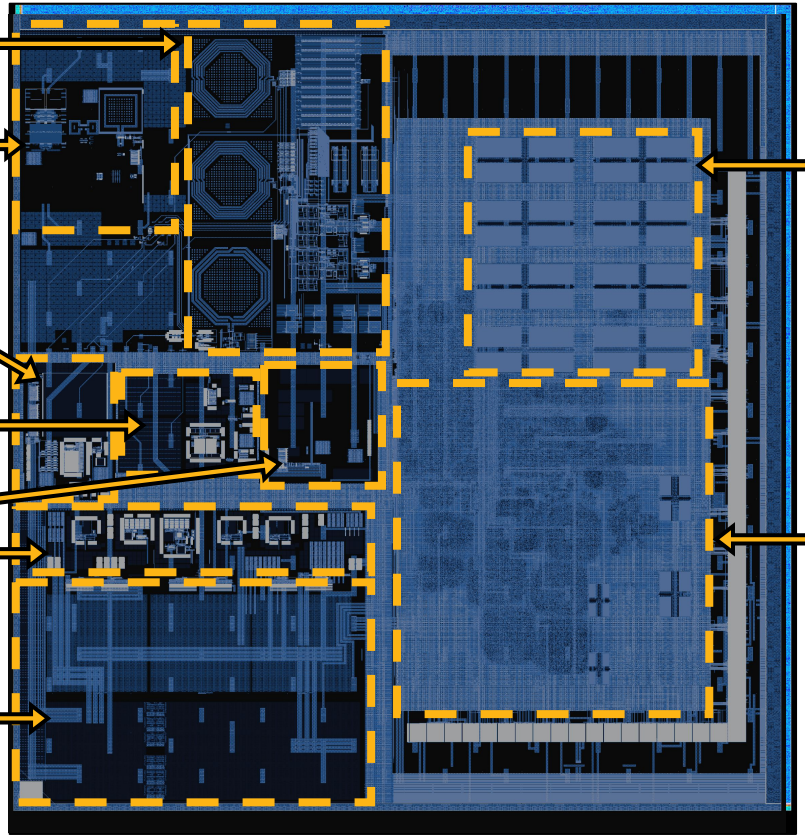
SCµM-V24 The 4th Gen "Analog-Heavy" Class Chip



2.4 GHz BLE & IEEE 802.15.4 Transceiver

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Booting Up Post Fabrication

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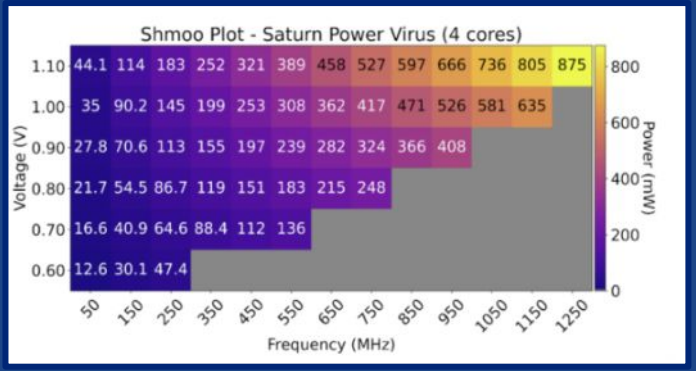
One Platform To ~~Rule~~ Bring Up Them All

We develop a suite of generalized tools for benchmarks + **full applications**.
Early TinyStories 260k Param LLaMa demo:

```
---- Sent utf8 encoded message: "5\n" ----
running llamaLet me tell you a story about computer. It's a beautiful lemonade
 to repair them and run into the park. He sees a big cup and a loud noise. It
was just a piece of chair. He sees a picture of a
```

IDE Baremetal-IDE



NeCTaR GIF, HotChips 2024
NeCTaR Peak: 1.28 tokens/sec

ShmooTester LIBBMARK

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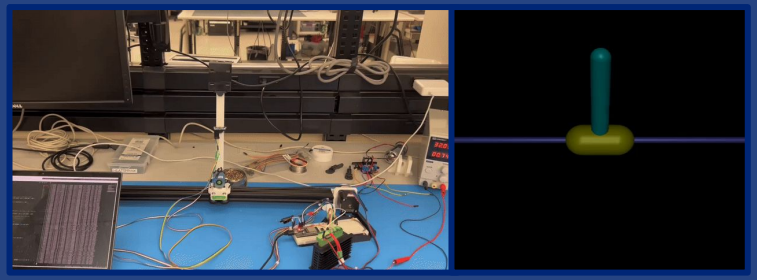
2-12x * Performance + Energy Efficiency in Physical

vs. Rocket Core

“How can you make use of silicon post-paper?”



Inverted Pendulum PD Control

Convolution

Centroid Recognition

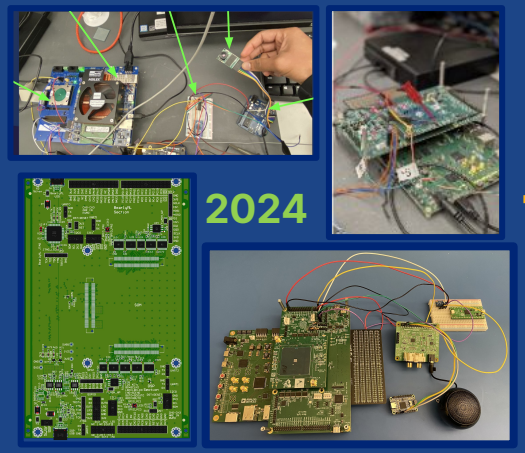
Click me!

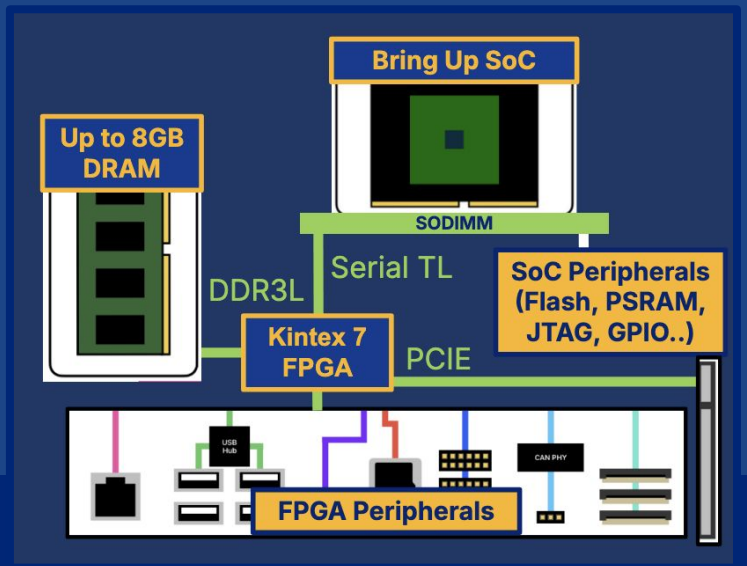
Bora Vision, Voice & AI

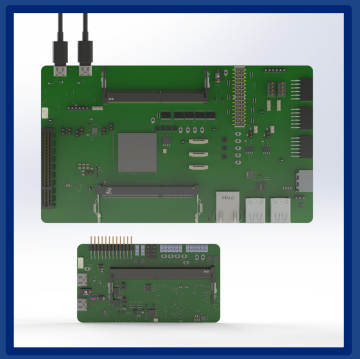
*For more benchmark + performance results see ESSERC 2025 talk.

Towards “One Cable Bring Up” For All Chipyard Chips

Now including hardware, we designed three generalizable platforms: BoraLake (book-sized), SophiaLake (small), DimaCove (tiny - robotics).







On-Board Clock, Power, FPGA..

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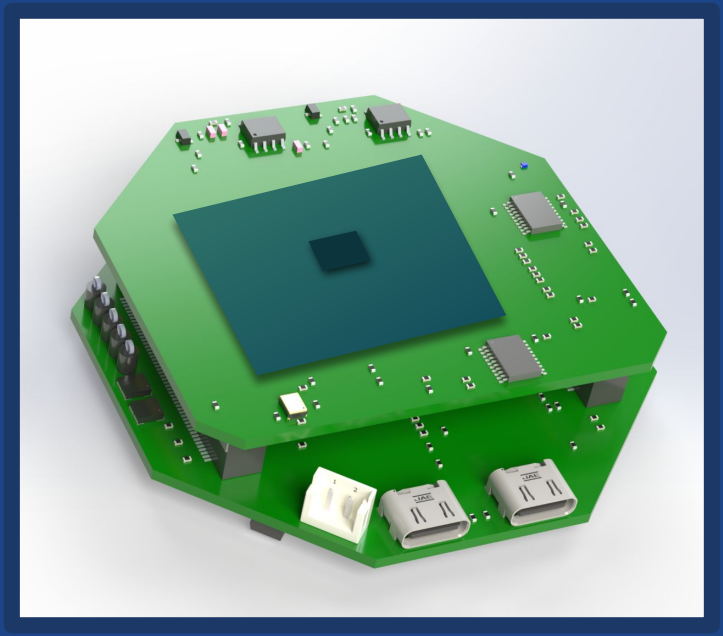
N. Zhao, J. Lomax et al.

“One Cable Bring Up” Realized



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Class Chips in LLM Action

COSMIC

Peak: 85.5 tokens/sec

Average: 23.8 tokens/sec

Efficiency: 1.1 mJ/token

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The Takeaways

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Agile Methodology is Training *the Future*, Making Valuable Contributions *Today*

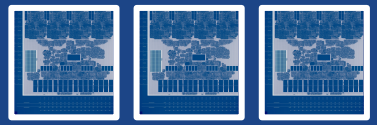
- Do not underestimate today's **open source silicon ecosystem.**
- **Chipyard** enables end-to-end silicon-proven **agile design + IP reuse.**
- Fast-paced, industry-relevant **TO classes** are reviving student interest.
  - Started in parallel a SKY130 fully student-run TO class*.
- Class chips - **COSMIC, MELLIS, SCμM-V** - compete with SoA SoCs.

We are always interested in new collaborations!

*https://151tapeout.berkie.ee/

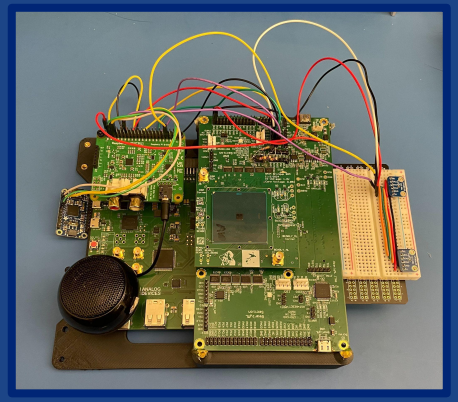
Want to know more? Come chat with us!

Featuring break time guests:



Once upon a time, there was a little girl named Lily. She loved to play in the park with her friends. One day, she went for a walk. She saw a big box with a pink coat that was gone. She was very sad. Lily wanted to make a big smile on her face. She asked her son, "What are you doing?" Her son said, "I want to play with it too, but I cannot make sure. Lily picked it up and said, "I'm going to jump in the sun As they were walking to the park

Story Time Bot



Parrot Bot

Spider Ant Bot

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The Faces Behind the “We”

UC Berk

Spring 2024 Tapeout Class & Friends

Acknowledgements

This project is the work of many in UC Berkeley's special topics chip tapeout and bring-up classes.

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Fun fact: MELLIS means honey!

UC Berkeley

SLICE

BWRC

Hot Chips 2025

Thank You
Q&A

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