

Specialized IC for World-Lock Rendering in Augmented and Mixed Reality Devices

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Orion combines the look and feel of a regular pair of glasses with the immersive capabilities of augmented reality – and it's the result of breakthrough inventions in virtually every field of modern computing.



Orion WLR Principles



WLR Experience



WLR Experience



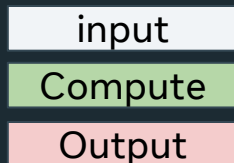
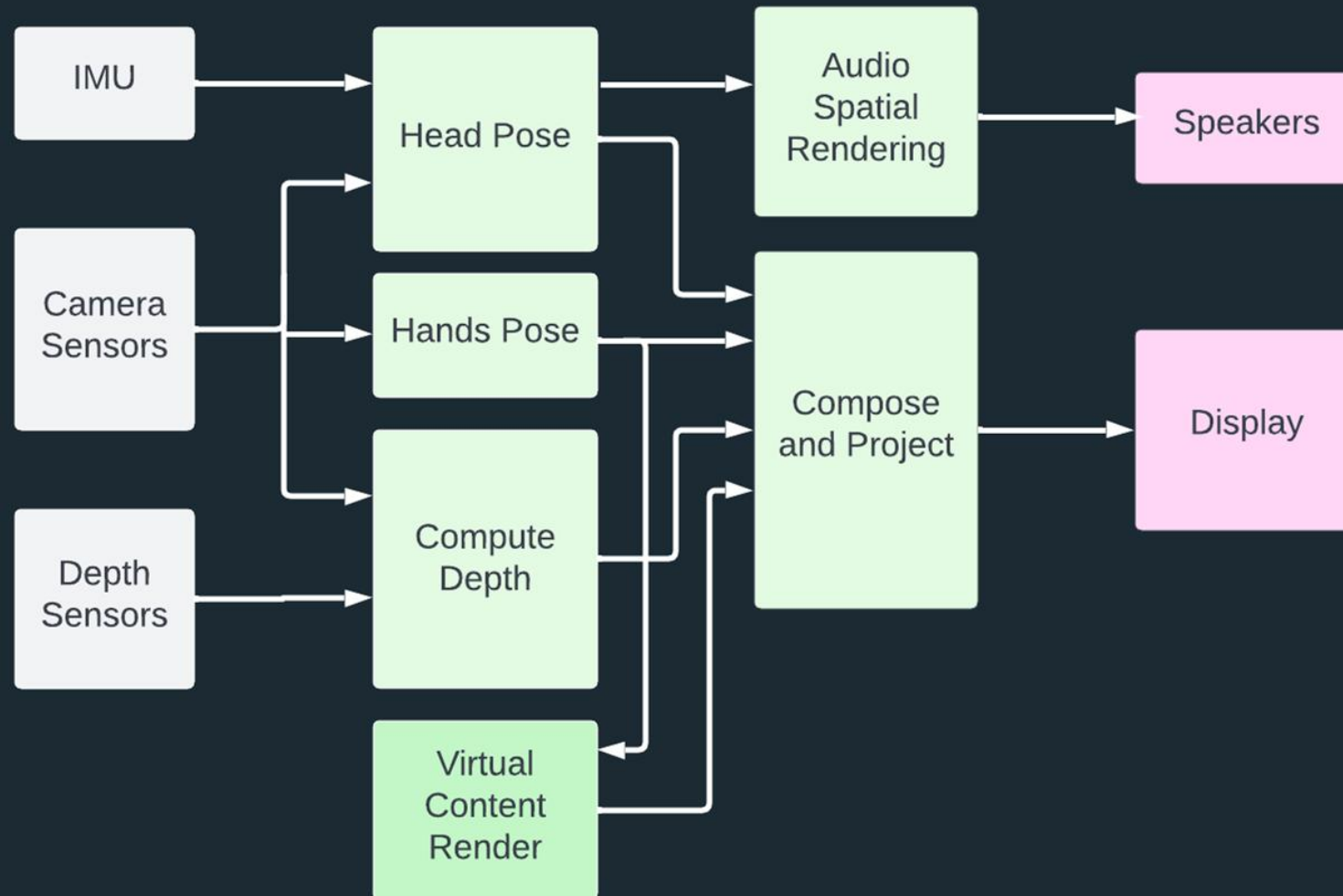
World Locked Rendering Principles

- Head Pose in 6 DOF
- Depth image of the scene
- Rendering the virtual augment
- Composing the scene, virtual and see-through
- Hand tracking and posing can be added as occluders and interaction
- Audio Spatial Rendering

Impacting the experience:

- Motion to Photon - latency from object or head movement to display update
- Power consumption & thermal dissipation

World Locked Rendering Block Diagram



Orion Glasses



Challenges to Solve with Silicon

Power

&

Size



Distributed Compute

- Advanced process node
 - Limit usage of DRAM
 - Fmax at Vmin
 - Aggressive power management
 - Compression
- Creative packaging
 - Minimize wire count

Compute Silicon in Orion



Glasses

Puck

Wrist

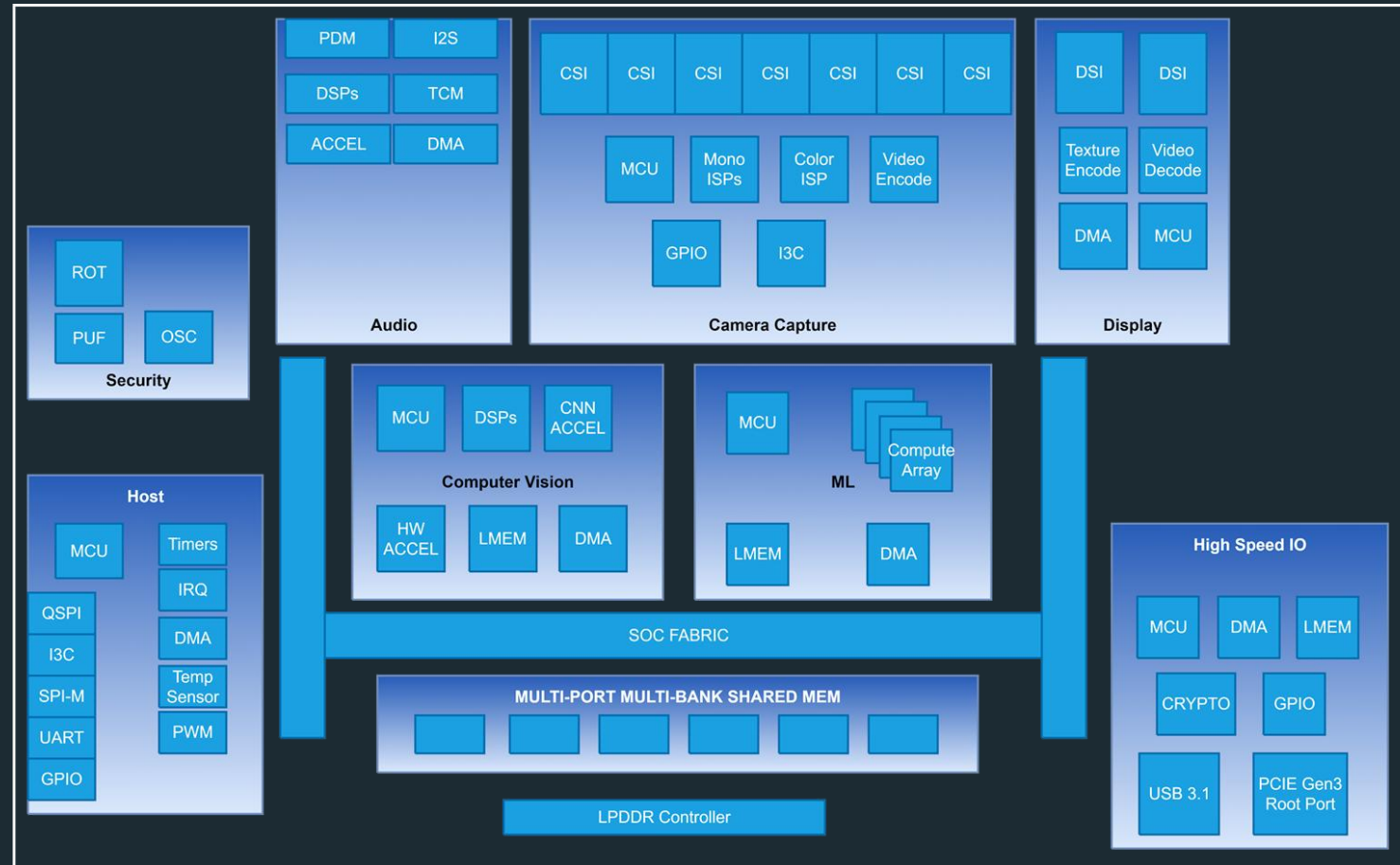
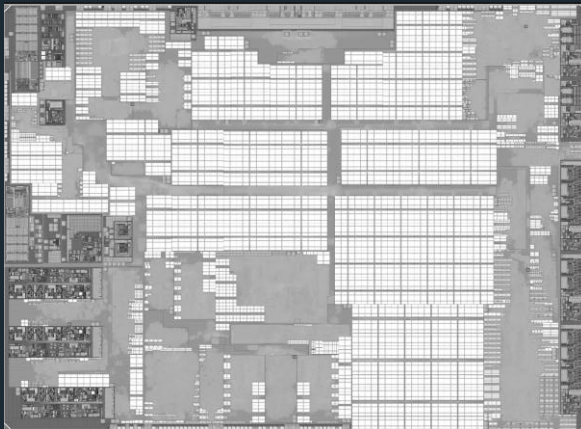


Architecture Considerations

- WLR pipeline is a continuous running workload
 - Unlike traditional burst-idle patterns
- Decentralized control
 - Ultra-low latency and aggressive power management
 - Simplified workload isolation and security
 - Modularity for future system partitioning
- Optionality and flexibility

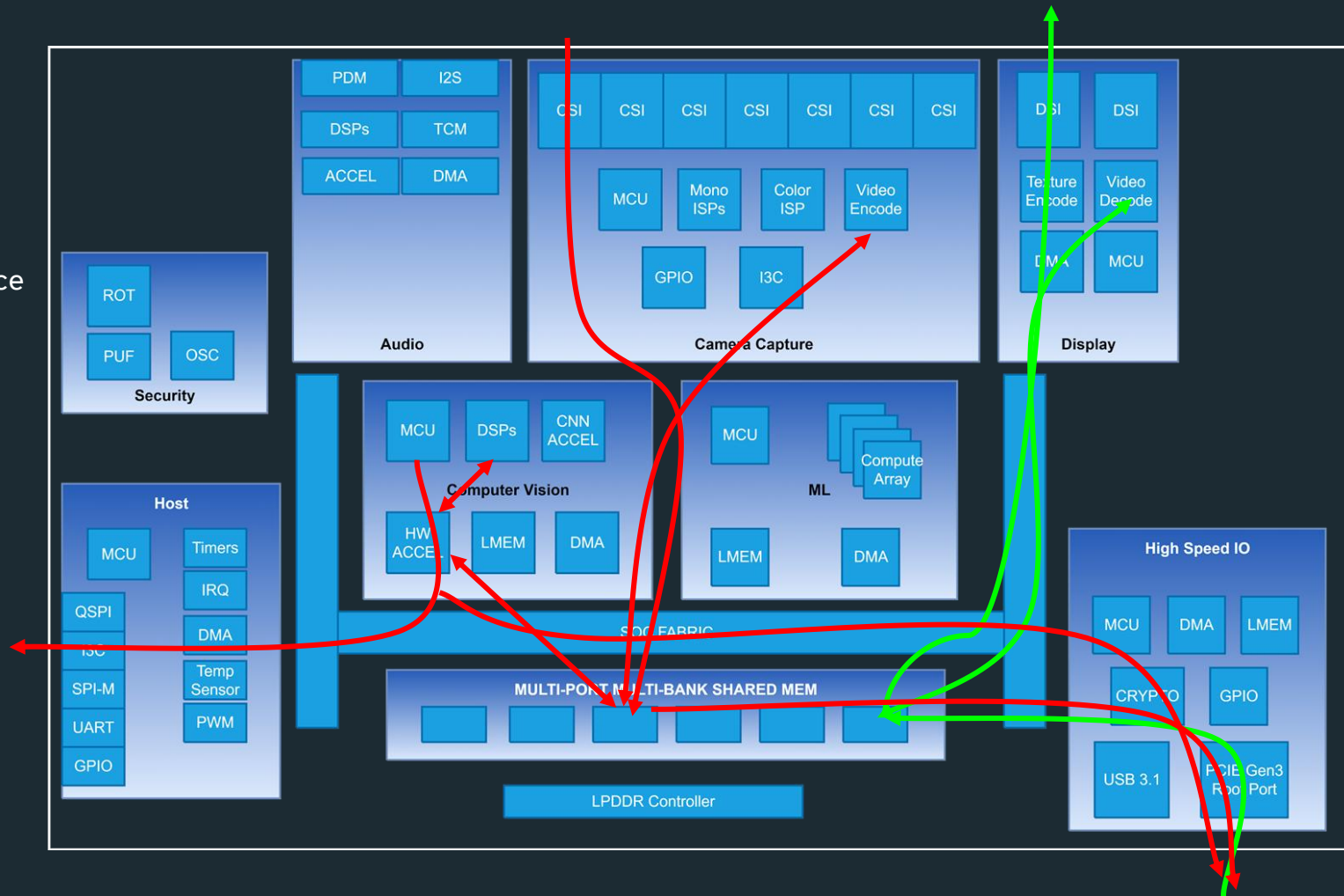
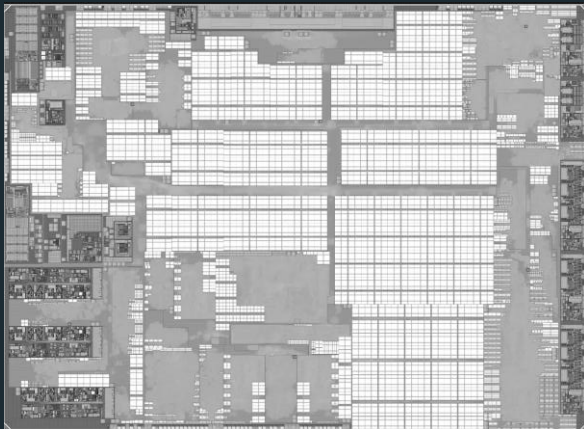
Glasses Processor

- Seven camera inputs
- ET and HT accelerator HW
- HEVC and custom compression
- Audio I/O
- Secure RoT and encryption/decryption
- Large on-die shared SRAM and LPDDR interface
- PCIe, USB, MIPI CSI Rx and DSI Tx
- SiP package combines:
 - SoC die
 - LPDDR4X
 - NVM Flash
- 2.4B transistors, 27 power domains
- 5nm process



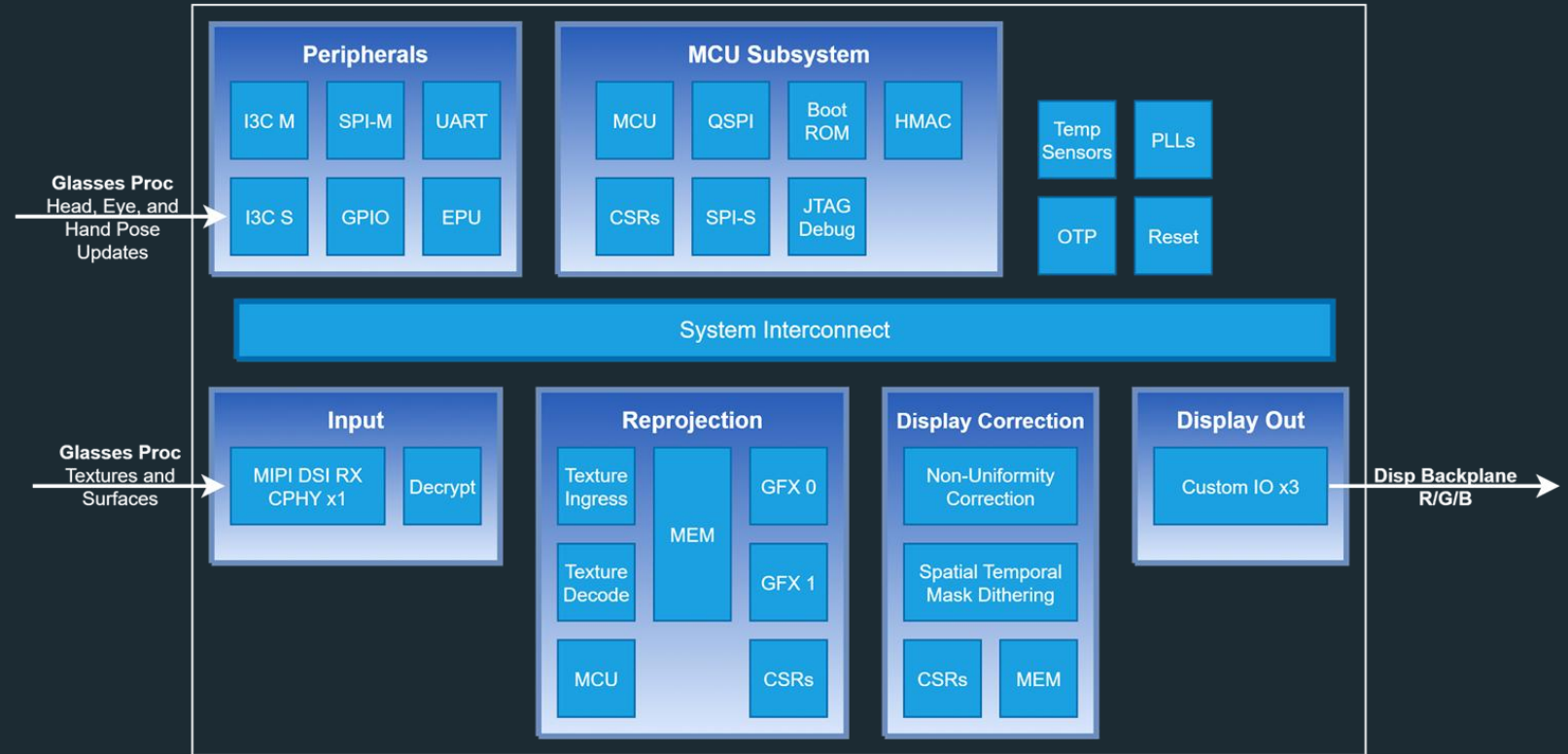
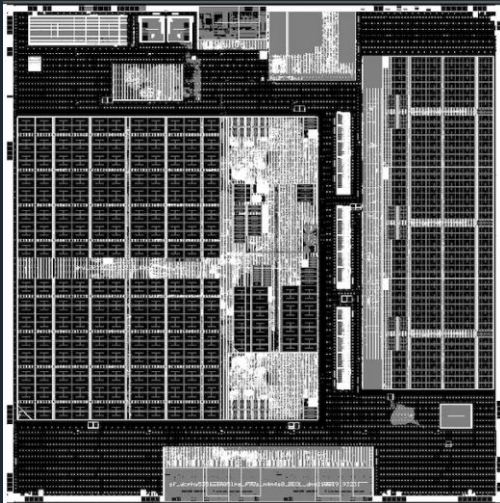
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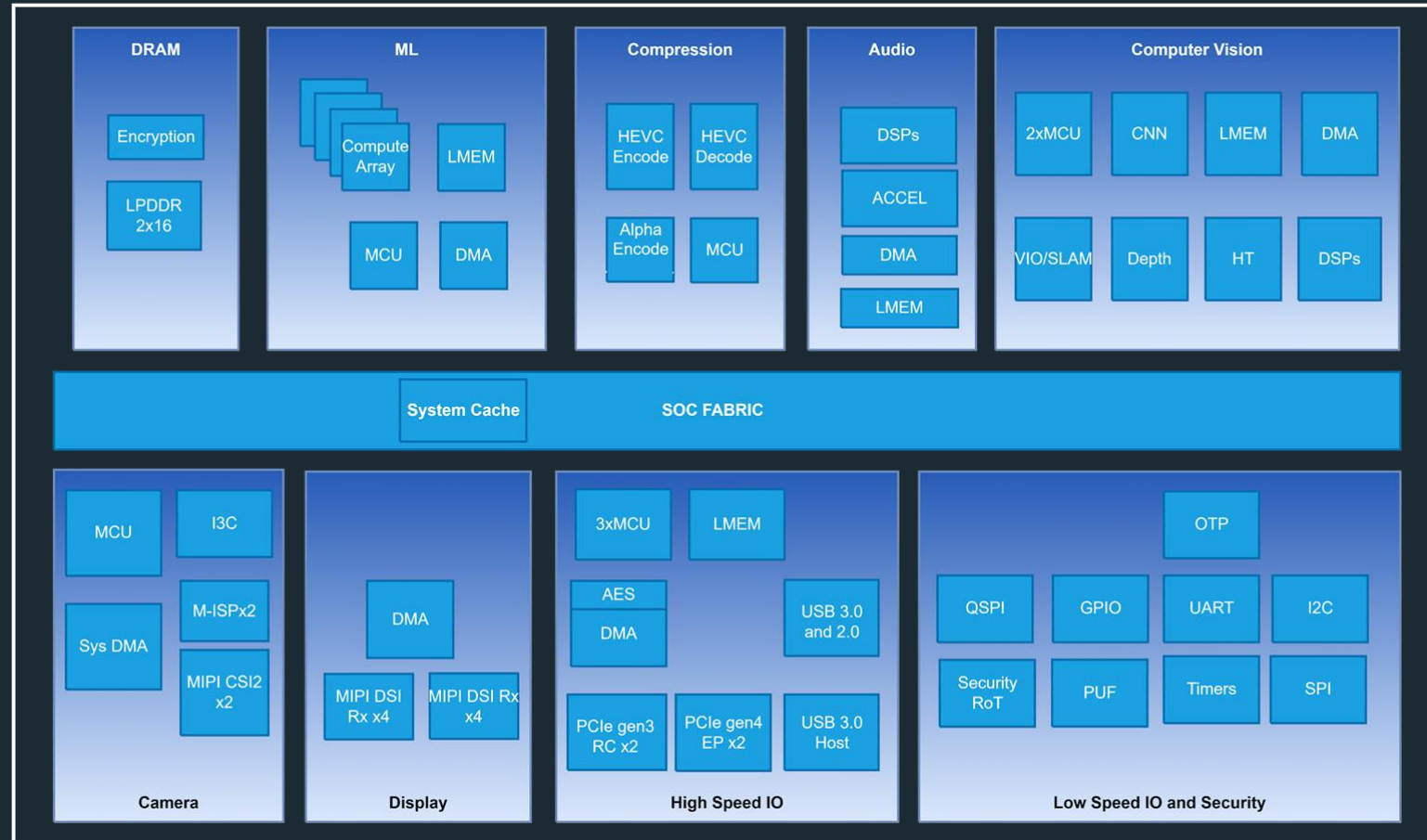
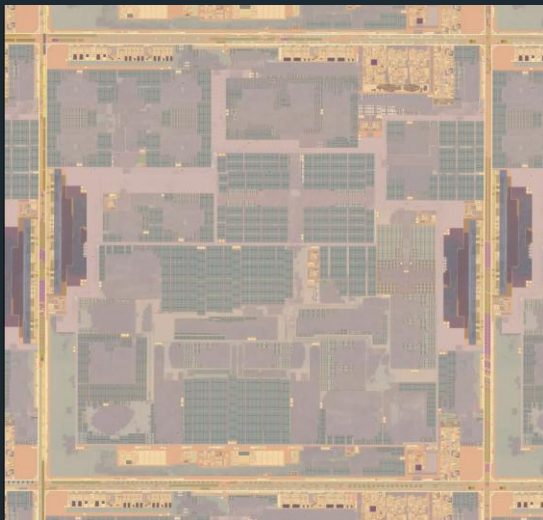
Display Processor

- Reprojection engine
- Display corrections
- Custom graphics compression
- Custom protocol over MIPI DSI Rx
- Large on-die SRAMs
- Co-packaged with display module
- 1.1B transistors, 9 power domains
- 5nm process



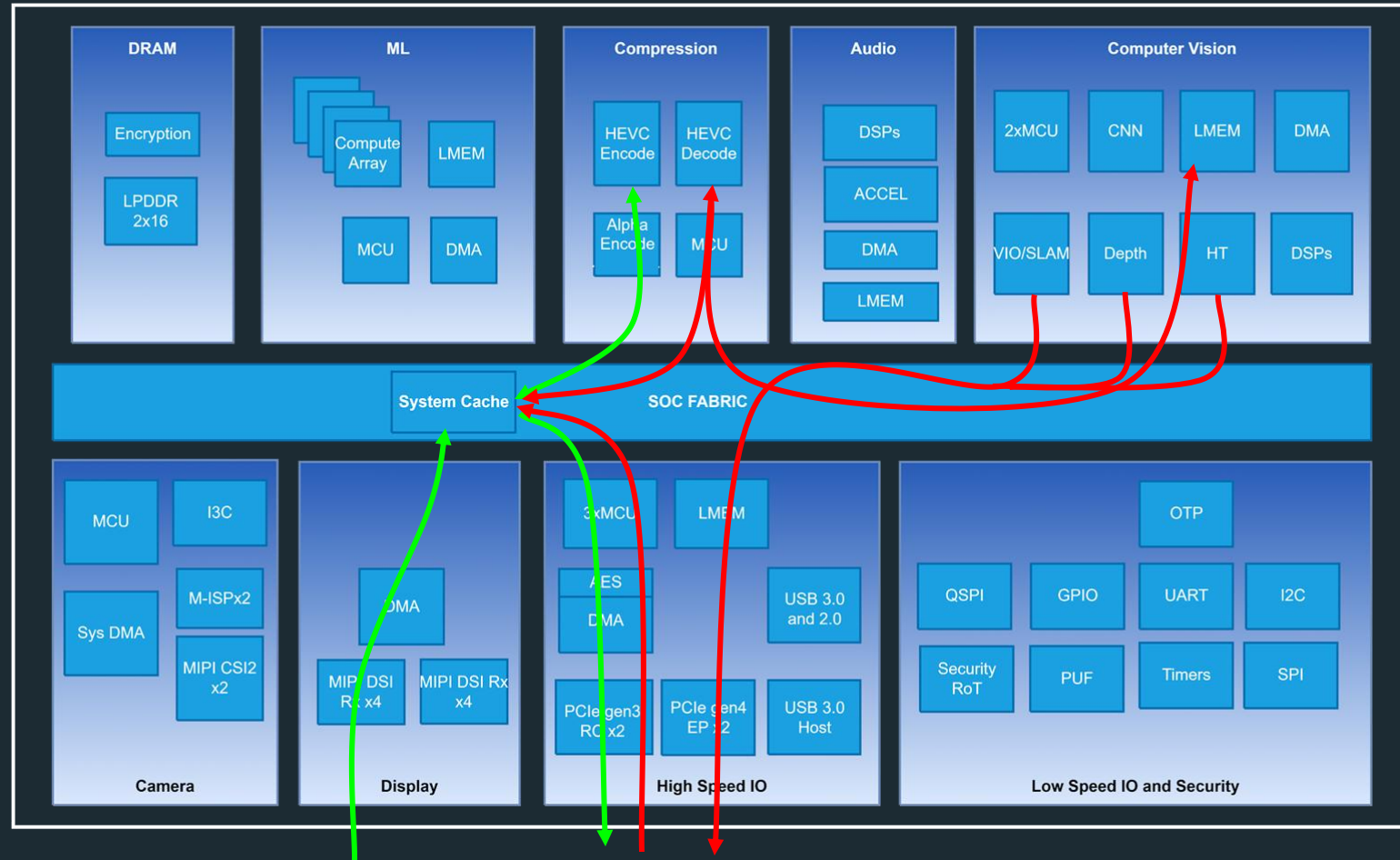
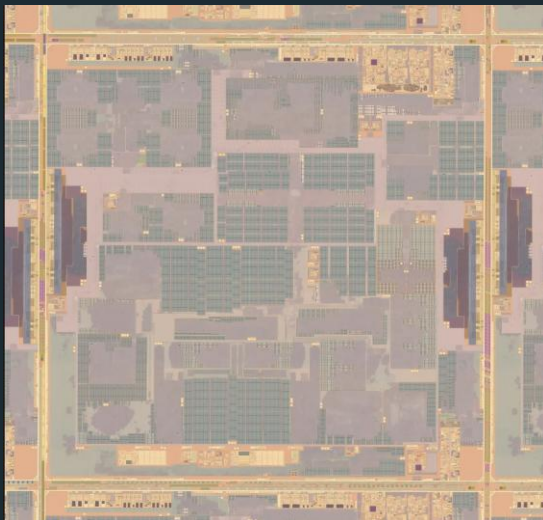
Compute Co-Processor

- CV processing (VIO/HT/Depth)
- ML engine
- Audio render and spatialization
- HEVC and alpha compression
- Large on-die SRAM and system cache
- Secure RoT and encryption/decryption
- PCIe, USB, CSI Rx and DSI Rx
- SiP package combines:
 - SoC die
 - LPDDR4X
- 5.7B transistors, 76 power domains
- 5nm process

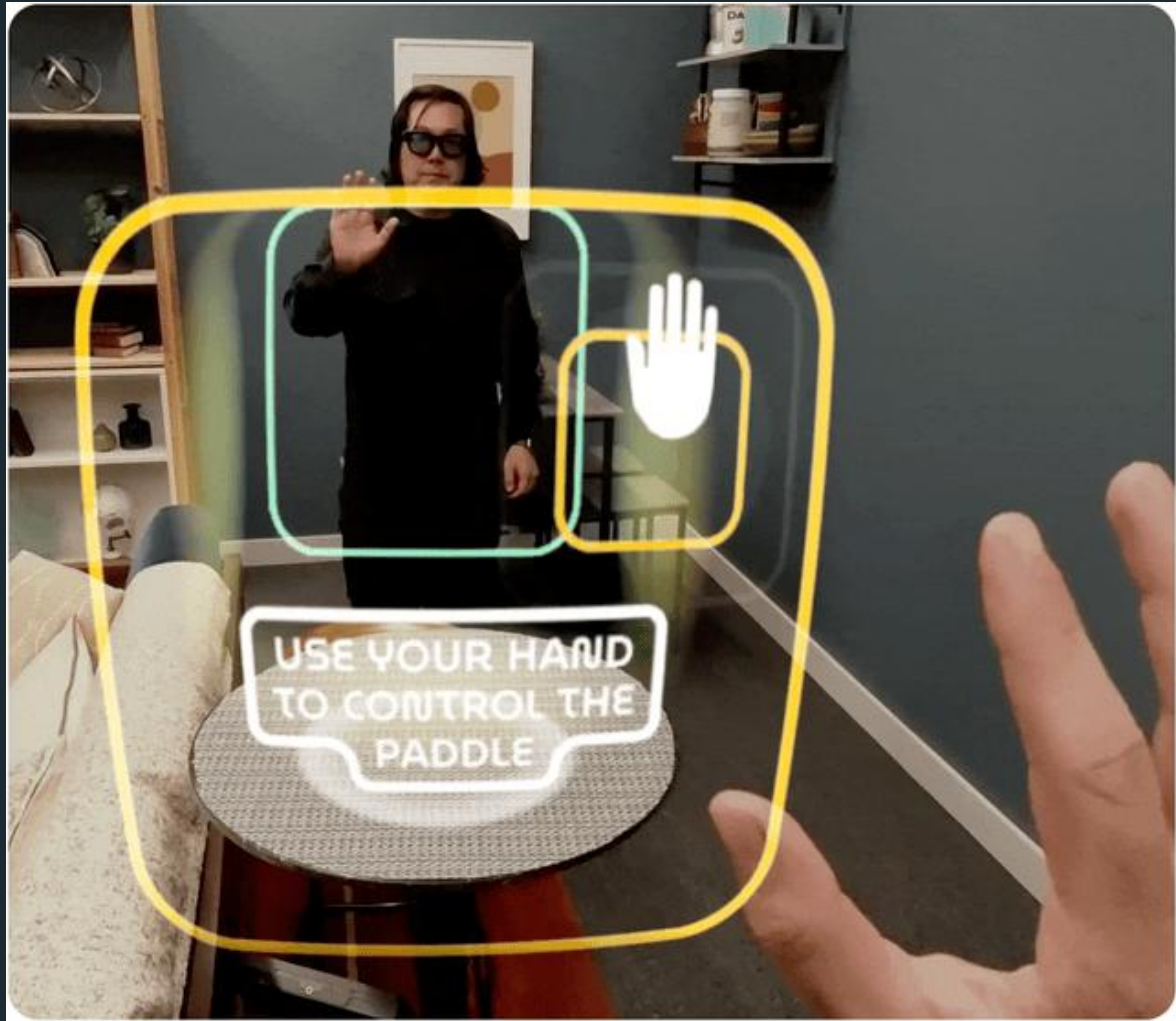


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Putting it all together



Thank You!

